ARTICLE

Maintaining SiC MOSFET Efficiency & Protection Without Compromise

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The efficiency and size benefits of SiC devices have been enthusiastically embraced by designers of industrial, automotive, traction systems and photovoltaic power conversion. To provide more detail, the lower sheet resistance of wide-bandgap SiC materials (typically 1/100th that of conventional silicon) results in smaller devices for a given current capacity—valuable in space-saving applications.

In addition, the electric-breakdown-field for SiC (approximately 2.8 MV/cm) allows for a much shorter isolation region within the material. A significant benefit is that the smaller size of SiC switches reduces parasitic capacitance, which improves switching efficiency and allows the switch to operate at higher frequency without penalty. These are clear benefits; however, the reduction in the mass of the switch means that protection circuitry must operate very quickly to prevent thermal damage. Shutdown in less than 3 µs is a common requirement for SiC devices (as compared to the 10 µs seen with conventional IGBT and MOSFET switches).

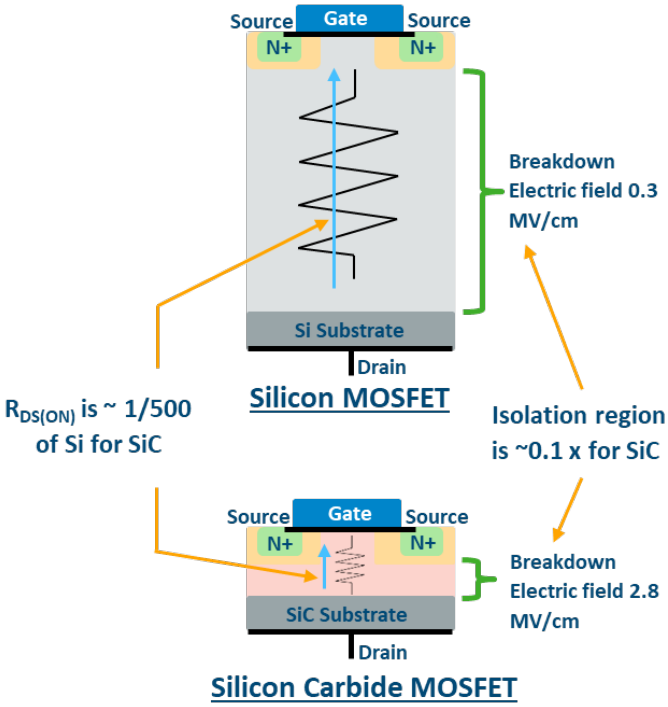
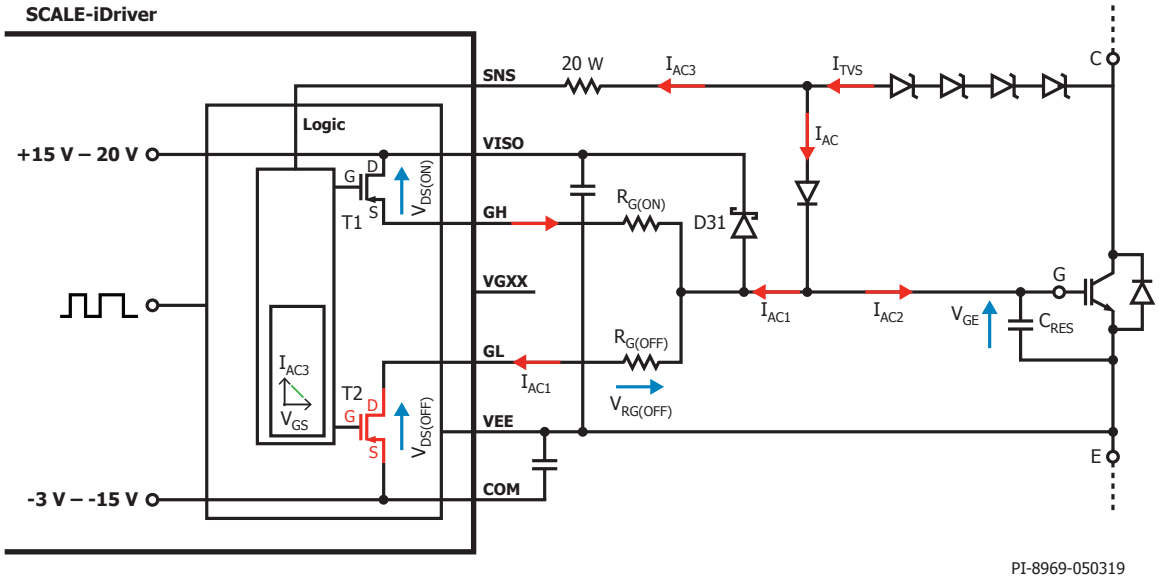


Figure 1: Comparing SiC with conventional silicon MOSFETs reveals the clearly superior semiconductor characteristics of the SiC material, which allows the construction of significantly smaller switching devices.

SiC technology is relatively new in the mainstream, and there are different device structures being used as MOSFET designers work the new material. Cascode and MOSFET configurations with different gate characteristics have resulted in a wide range of gate voltage requirements, further challenging the circuit designer. As with all switches, protection circuitry is required to safely turn off the switch in the event of a system short-circuit. Desaturation detection must avoid false tripping, and this typically results in a switch blanking time of up to 2 µs—a significant portion of the thermally-limited, high-current time envelope. Fast turn off (rapid di/dt) may induce V_{DS} overvoltage during shutdown, so shutdown rate must also be controlled.

Figure 2 shows a typical gate drive circuit for an IGBT switch and associated short-circuit shutdown characteristic. During a short-circuit shutdown, V_{CE} rises above the DC Link voltage and causes the TVS network to break over delivering current I_{AC} to the gate node. I_{AC2} charges C_{RES} and causes the gate voltage to rise and turn the switch back on to limit V_{CE} , However switch T2 pulls current $I_{AC1THRU}$ gate resistor $R_{G(OFF)}$. Increasing I_{AC3} (via ACL pin) increases the impedance of T2 and reduces I_{AC1} , but this takes time. The solution is to increase the gate resistance, which will reduce the current drain from the gate node and improve the clamping voltage. Driving and IGBT in this way is effective, and the change in gate resistance does not significantly change switch efficiency. However, increasing gate resistance for a MOSFET will reduce switch transition speed, increase switching losses and reduce efficiency.



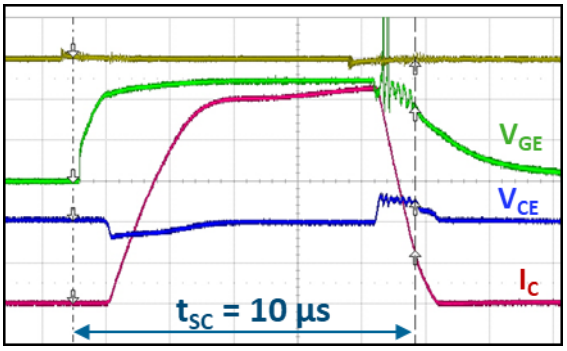
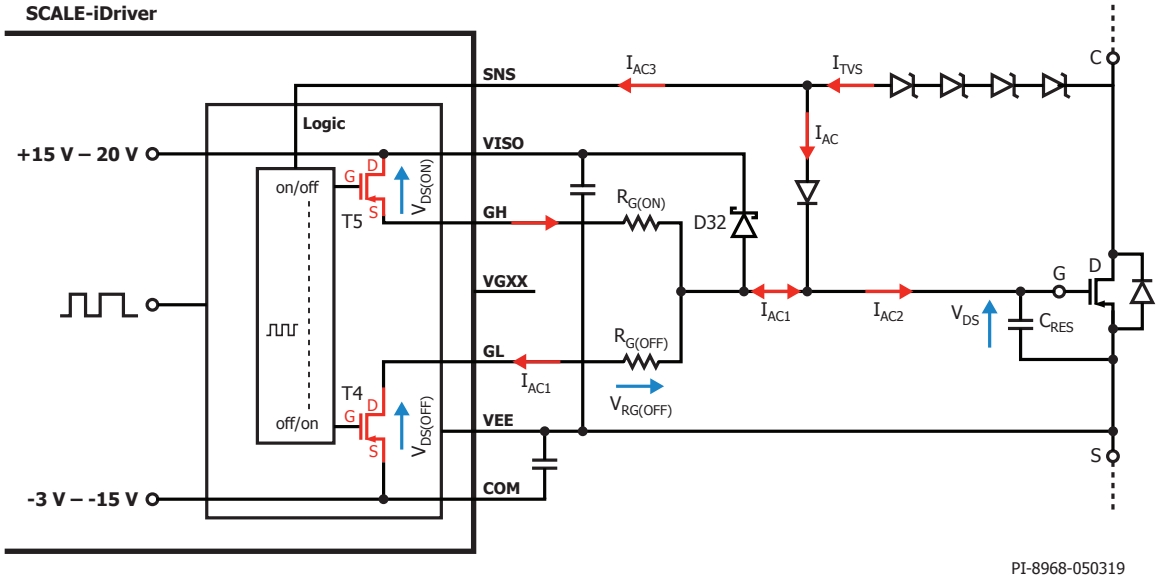


Figure 2: IGBT desaturation detection and advanced soft shutdown in operation. I_C increases and induces a shutdown (V_{GE} reducing). Subsequent overvoltage (V_{CE}) detection causes an increase in V_{GE} to limit voltage overshoot and complete a safe shutdown of the switch by limiting di/dt.

To safely and quickly shut down an SiC switch without increasing gate resistance requires a different detection and shutdown strategy. Figure 3 Shows an SiC switch short-circuit shutdown using a new control algorithm to provide rapid and controlled switch shutdown.

As before, the desaturation triggered shutdown induces a V_{DS} overvoltage to occur, this causes the TVS stack to break over. I_{AC2} charges C_{RES}. As before, I_{AC1} begins to flow thru $R_{G(OFF)}$ reducing I_{AC2}. However, in this configuration I_{AC3} induces a rapid response from the IC control logic. In this case, the control circuitry rapidly toggles T4 and T5 to alternately sink and source I_{AC1} current. This strong drive reduces the effect of $R_{G(OFF)}$ on I_{AC2} , making an adjustment in gate resistance unnecessary. This allows fast turn-off and control of V_{DS} without compromising efficiency.



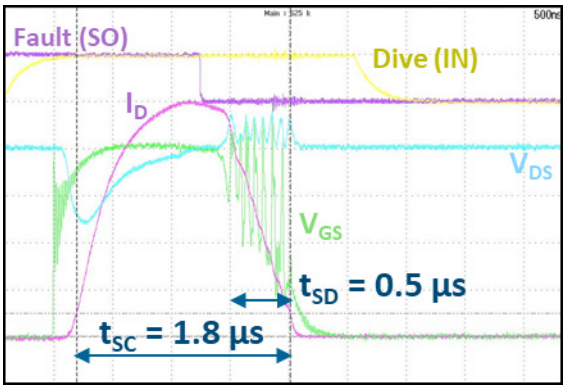


Figure 3: SiC advanced active clamping: Toggling current to the gate via T4 and T5 provides a very rapid shutdown while providing an aggresive control of V_{GS} to limit the V_{DS} excursion. Following a 1.3 µs blanking time, a desturation-fault shutdown asserts, allowing the SiC MOSFET to be turned off in less than 1.8 µs. The toggling of the V_{GS} gate drive can be clearly seen.

By removing the role that the gate resistors play in limiting voltage overshoot, the SiC advanced active clamping employed in the SiC SCALE-iDriver IC family from Power integrations allows the designer to optimize the gate drive resistors to maximize efficiency without compromising performance to insure safe shutdown protection.

How is the gate driving challenge being addressed?

Figure 4 shows typical gate voltage regions for different SiC switch structures. Some devices require a regulated turn-on voltage, while others need a regulated negative turn-off voltage to ensure that they do not exceed the gate-source safe operating area as given in their respective data sheets. Typically, only one voltage can be regulated, while the other voltage is dependent on actual load conditions.

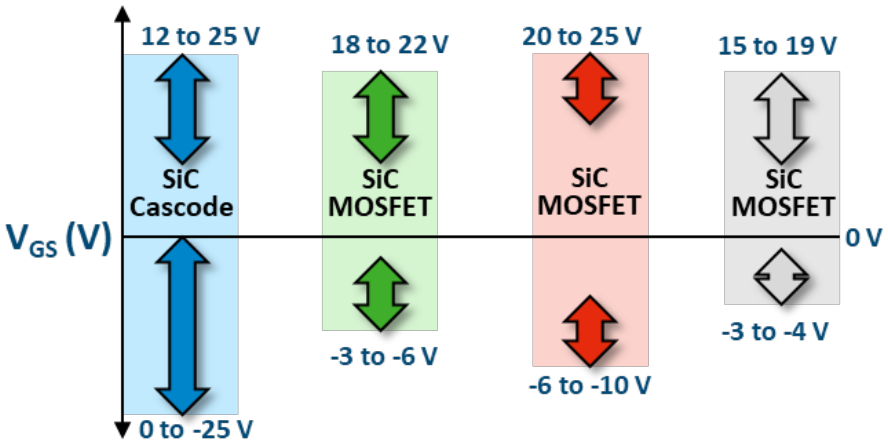


Figure 4: Turn-on and turn-off requirements for different SiC switch types. The requirements are often mutually exclusive—making the design of the 'universal SiC gate driver' more challenging.

To create a stable gate-driver control voltage, various controllers use bi-polar or unipolar supply voltages to provide an isolated driver voltage. A unipolar-based gate driver is shown in Figure 5. The power supply delivers a raw supply voltage to the VISO pin of the control IC. To match the requirements of a particular SiC MOSFET, an external programming input is required. A gate driver bias circuit is used to adjust the center point of the drive rails (delivered via the GH and GL pins). A potential divider between VISO and COM pins is used, together with a shunt regulator to control the drive voltage partitioning via the VEE pin. The shunt regulator provides a more stable temperature and load voltage than would a simple Zener diode solution.

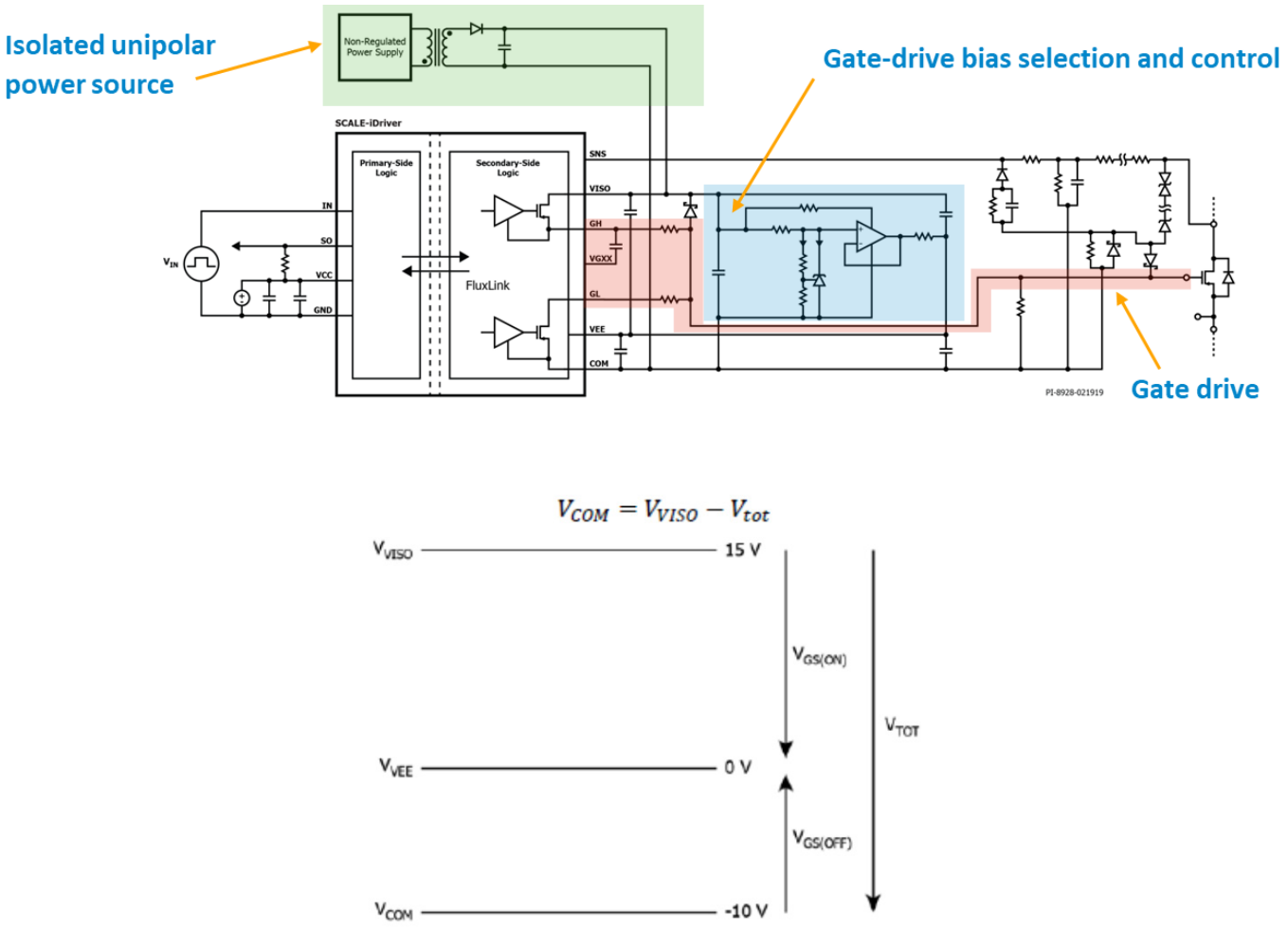


Figure 5: A SCALE-iDriver power transformer provides 15 V to the VISO pin and the control IC uses an internal regulator to generate a stable drive voltage, as directed by the bias input. Additional circuit modifications may be required to reduce potential circuit oscillations during turn-on which will be switch dependent (see AN-1601 at power.com for more information).

Driving silicon carbide MOSFETs provides significant challenges for the gate-driver circuitry. Traditional control techniques are often inadequate—unable to support the rapid switching and corresponding overvoltage control issues that follow a desaturation (short-circuit) event. In addition, the nascent nature of SiC switch design means that there is wide variation in gate-drive voltage requirements. Solutions exist that can provide the rapid control and meet programmability without compromising efficiency or safety in switching circuits.

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