Design Example Report

Title	*50 W Power Supply Using InnoSwitch™3-EP PowiGaN™ INN3679C-H606*
Specification	90 VDC – 150 VDC Input; 12 V / 4.16 A Output
Application	Solar Race Car Auxiliary Power Supply
Author	Applications Engineering Department
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Summary and Features

- InnoSwitch3-EP is industry first AC/DC IC with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
- Insensitive to transformer variation
- Built-in synchronous rectification for high efficiency
- Full load operation from 90V_{DC} to 150 V_{DC}
- Primary sensed overvoltage protection
- Very low component count: 36 components
- Internal short-circuit protection
- Very high efficiency at different loads
- Average of 95.7% from 30% to 70% load at 120 V_{DC}
- Very high full-load efficiency
- 95.22% at 120 V_{DC}

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1 Introduction

This document is an engineering report describing a 12 V / 4.16 A output power supply intended to be used as an auxiliary power supply for a solar race car. The design supports an input range of 90 VDC to 150 VDC.

This design uses the 750 V rated PowiGAN switch INN3679C from the InnoSwitch3-EP family of ICs in a flyback converter configuration; made by modifying RDR-747.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

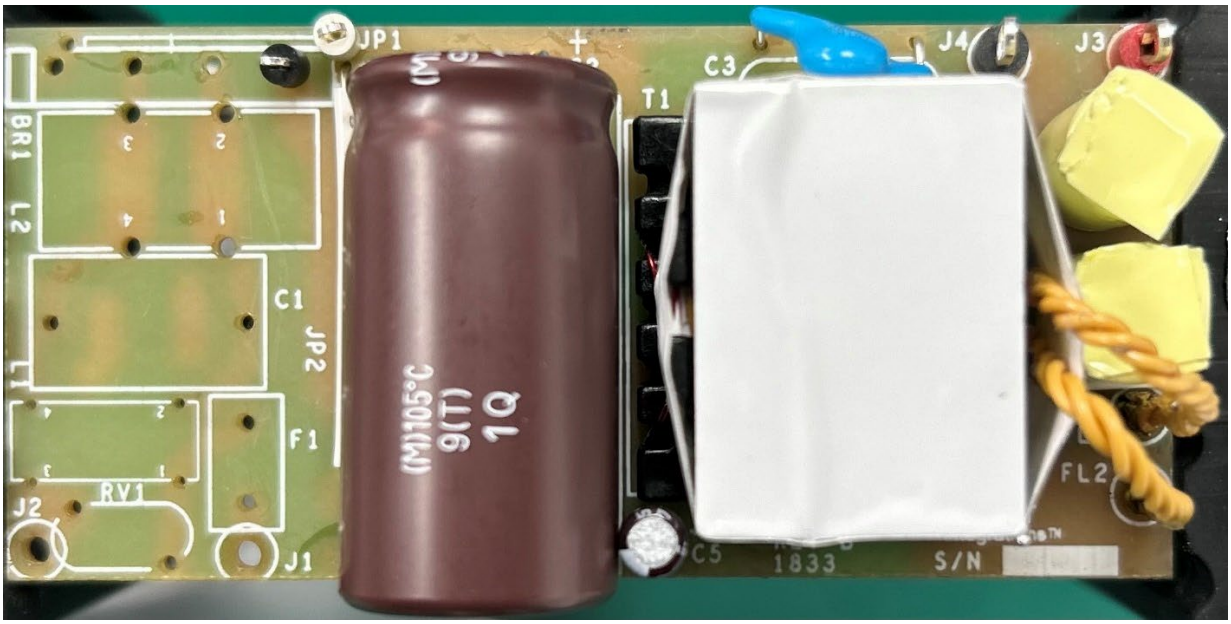


Figure 1 – Populated Circuit Board Photograph, Top.

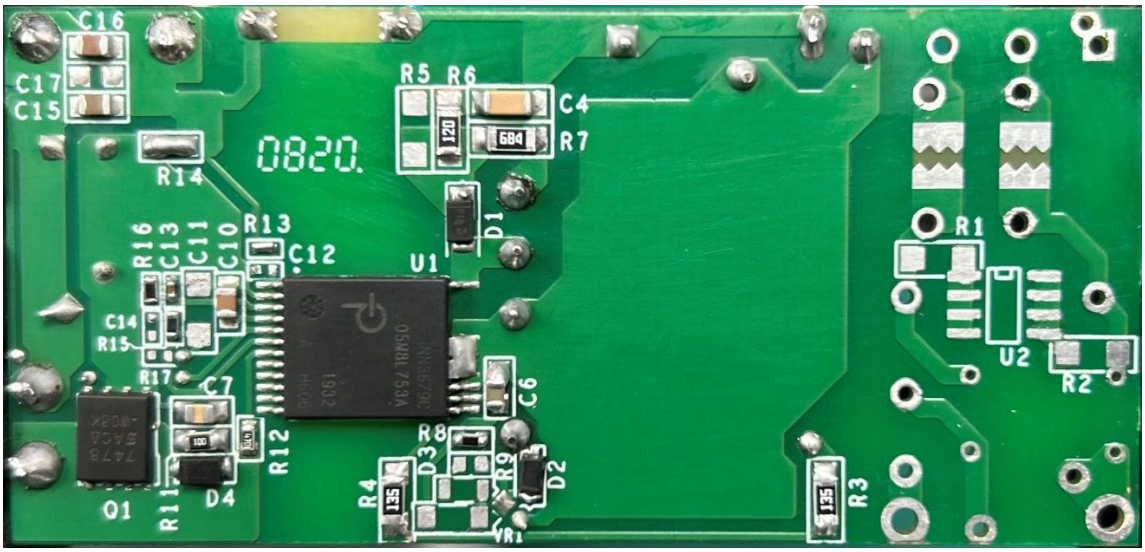


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the result section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input Parameters						
Voltage	V_{IN}	90	120	150	VDC	
Output Parameters						
Output Voltage	V_{OUT1}		12		V	±5%
Output Ripple Voltage	$V_{RIPPLE1}$			300	mV	On Board.
Output Current	I_{OUT1}			4.16	A	On Board.
Continuous Output Power	P_{OUT}			50	W	
Operating Temperature						
Ambient Temperature	T_{AMB}	0		50	°C	Open Frame, Sea Level.

3 Schematic

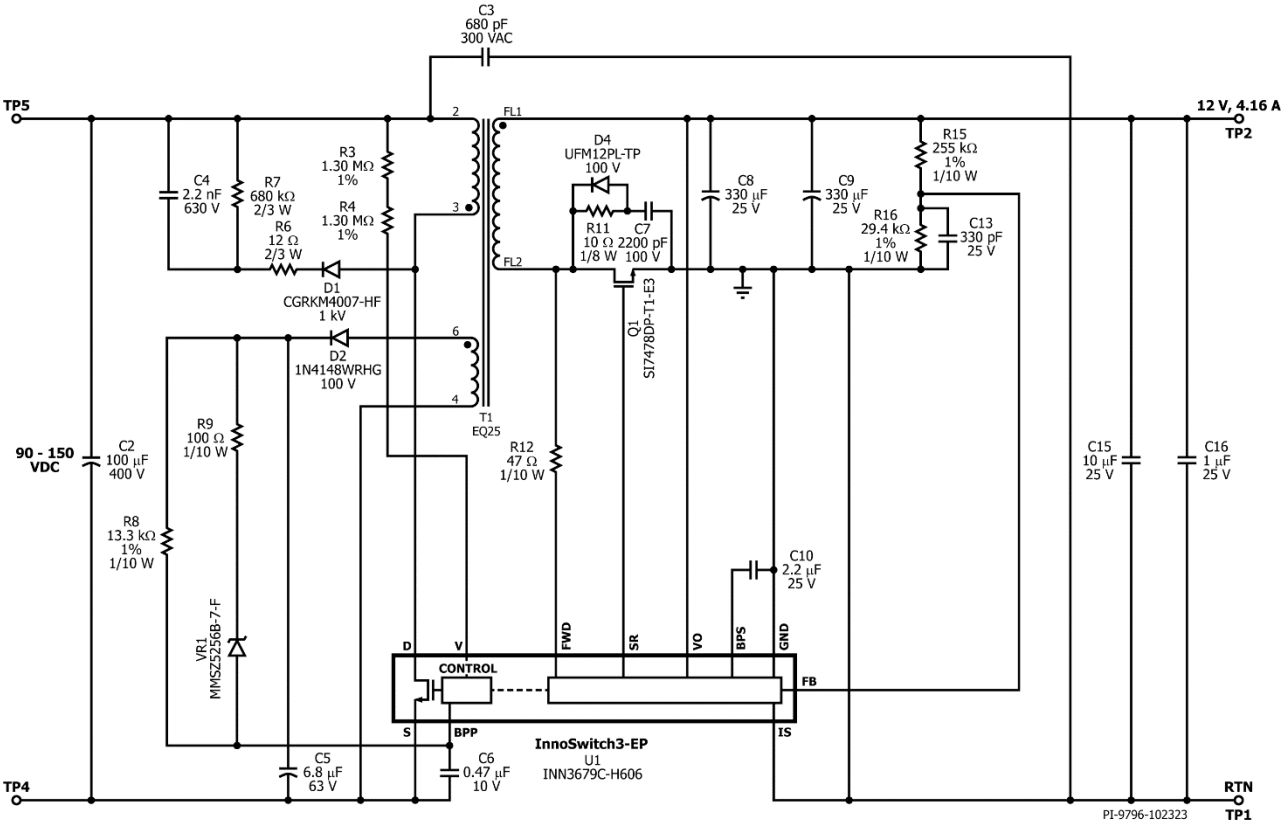


Figure 3 – Power Stage Schematic.

4 Circuit Description

4.1 InnoSwitch3-EP IC Primary

One end of the transformer (T1) primary is connected to the input DC bus filtered by input capacitor C2; the other is connected to the drain terminal of the switch inside the InnoSwitch3-EP IC (U1). Resistors R3 and R4 provide input voltage sense protection for undervoltage and overvoltage conditions.

A low-cost RCD clamp formed by diode D1, resistors R6, and R7, and capacitor C4 limits the peak drain voltage of U1 at the instant of turn-off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

The IC is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when DC input is first applied. During normal operation the primary-side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-EP IC (U1).

Zener diode VR1 along with R9 offers primary sensed output over voltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of over voltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1 which then causes a current to flow into the BPP pin of InnoSwitch3-EP IC U1. If the current flowing into the BPP pin increases above the I_{SD} threshold, the InnoSwitch3-EP controller will latch off and prevent any further increase in output voltage.

4.2 InnoSwitch3-EP IC Secondary

The secondary-side of the InnoSwitch3-EP IC monitors the output voltage and is responsible in driving the MOSFET providing synchronous rectification. The secondary of the transformer is rectified by MOSFET Q1 and filtered by capacitors C8 and C9. High frequency ringing during switching transients that would otherwise create radiated EMI is reduced via an RCD snubber R11, C7 and D4. Diode D4 was used to minimize the dissipation in resistor R11.

The gate of Q1 is turned on by secondary side controller inside IC U1, based on the winding voltage sensed via resistor R12 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 3 mV. The secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

The secondary-side of the IC is self-powered from either the secondary winding forward voltage or the output voltage. Capacitor C10 connected to the BPS pin of InnoSwitch3-EP IC U1 provides decoupling for the internal circuitry.

During constant voltage mode operation, output voltage regulation is achieved through sensing the output voltage via divider resistors R15 and R16. The voltage across R16 is fed into the FB pin with an internal reference voltage threshold of 1.265 V. Output voltage is regulated by maintaining a voltage of 1.265 V on the FB pin. Capacitor C13 provides noise filtering of the signal at the FB pin.

The capacitors C15 and C16 are used to reduce the high frequency output voltage ripple.

5 PCB Layout

PCB copper thickness is 2.0 oz.

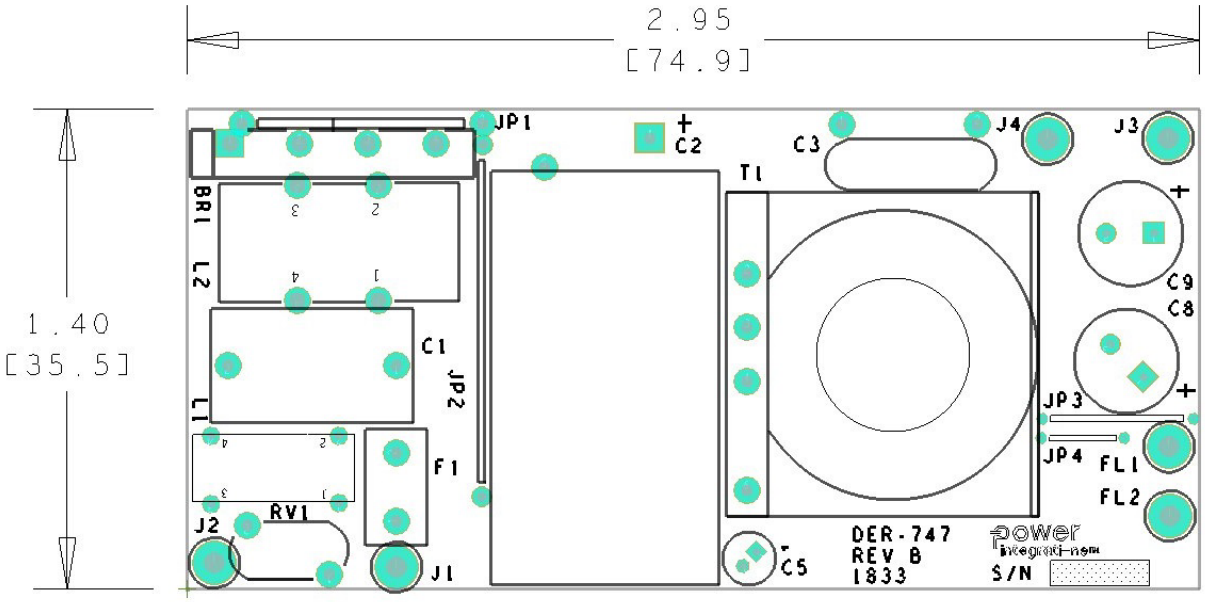


Figure 4 – Printed Circuit Layout, Top.

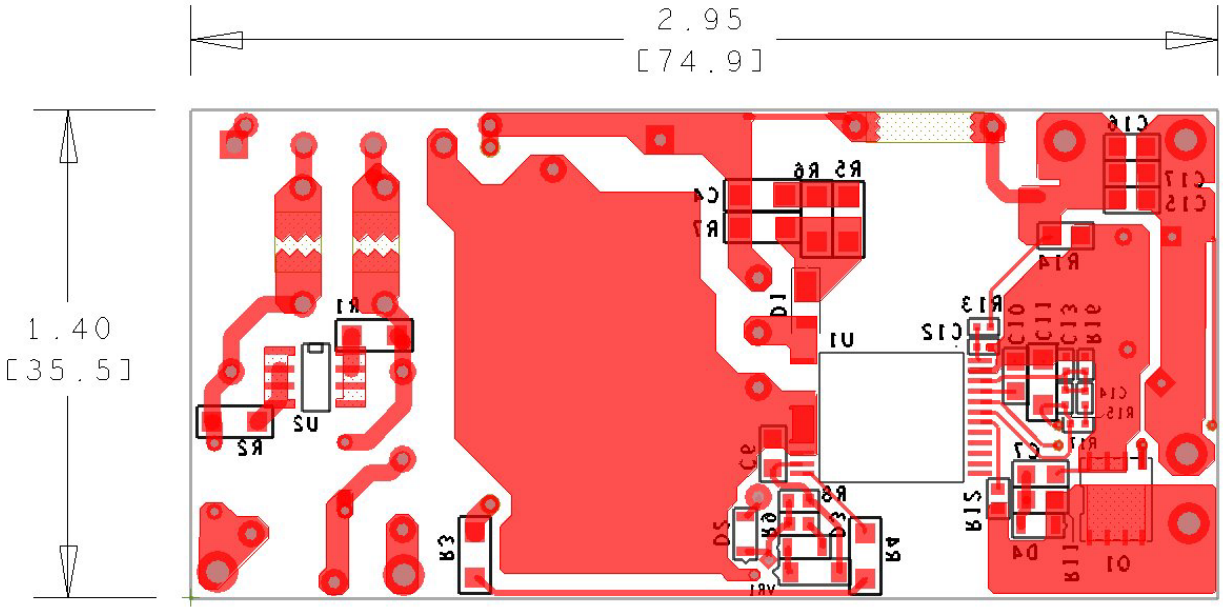


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	C2	100 uF, 400 V, Electrolytic, Low ESR, (16 x 30)	EPAG401ELL101ML30S	Nippon Chemi-Con
2	1	C3	CAP, CER, 680pF, ±10% , 300VAC, X1, Y1, B Radial, Disc,0.315" Dia (8.00mm),0.433" H(11.00mm),0.394" LS(10.00mm)	DE1B3KX681KA4BP01F	TDK
3	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK Corp
4	1	C5	6.8 uF, ±20%, 63 V, Electrolytic, Gen Purpose, (4mm x 11mm)	UPW1J6R8MDD6	Nichicon
5	1	C6	0.47 µF, ±5%, 10V, Ceramic Capacitor X7R, 0805 (2012 Metric)	VJ0805Y474JXQTW1BC	Vishay Vitramon
6	1	C7	2200 pF, ±10%, 100V, Ceramic Capacitor X7R, 0805 (2012 Metric)	CC0805KRX7R0BB222	Yageo
7	2	C8 C9	330 uF,±20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 mOhm, 2000 Hrs @ 105°C, (8mm x 13mm	A750KS337M1EAAE018	KEMET
8	1	C10	2.2 uF, 25 V, Ceramic, X7R, 1206	TMK316B7225KL-T	Taiyo Yuden
9	1	C13	330 pF, ±10%, 25V, Ceramic Capacitor, X7R, 0402 (1005 Metric)	04023C331KAT2A	AVX
10	1	C15	10µF ±10% 25V Ceramic Capacitor X7S 0805 (2012 Metric)	C2012X7S1E106K125AC	TDK
11	1	C16	1 uF, ±10%, 25 V, Ceramic, X7R, 0805 (2012 Metric)	GCM21BR71E105KA56L	Murata
12	1	D1	1000 V, 1 A, General Purpose, Standard Recovery >500ns, > 200mA (Io), SOD123F	CGRKM4007-HF	Comchip
13	1	D2	DIODE, GEN PURP, 100V, 150MA, SOD123, SOD-123F	1N4148W RHG	Taiwan Semi
14	1	D4	100V, 1 A, Fast Recovery, SOD-123FL	UFM12PL-TP	Micro Commercial
15	1	JP2	Wire Jumper, Insulated, 24 AWG, 1.0 in	C2003A-12-02	Gen Cable
16	1	JP3	Wire Jumper, Insulated, 28 AWG, 0.5 in	2842/1 WH005	Alpha Wire
17	1	JP4	Wire Jumper, Insulated, 28 AWG, 0.3 in	2842/1 WH005	Alpha Wire
18	1	Q1	60 V, 15 A, N-Channel, PowerPAK SO-8	SI7478DP-T1-E3	Vishay
19	2	R3 R4	RES, 1.30 M, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF1304V	Panasonic
20	1	R6	RES, 12 R, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J120V	Panasonic
21	1	R7	RES, 680 k, 5%, 2/3 W, Thick Film, 1206	ERJ-P08J684V	Panasonic
22	1	R8	RES,13.3 kOhms ±1% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603FR-0713K3L	Yageo
23	1	R9	RES,100 Ohms ±5% 0.1W, 1/10W Chip Resistor 0603 (1608 Metric) Moisture Resistant Thick Film	RC0603JR-07100RL	Yageo
24	1	R11	RES, 10 R, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ100V	Panasonic
25	1	R12	RES, 47 R, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
26	1	R15	RES, 255.0 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2553X	Panasonic
27	1	R16	RES, 29.4 k, 1%, 1/10 W, Thick Film, 0402	ERJ-2RKF2942X	Panasonic
28	1	T1	Bobbin, EQ25, 6 pins, 6pri, 0sec	POT-2501	Shenzhen xin yu jia
29	2	TP1 TP4	Test Point, BLK,THRU-HOLE MOUNT	5011	Keystone
30	1	TP2	Test Point, RED,THRU-HOLE MOUNT	5010	Keystone
31	1	TP5	Test Point, WHT,THRU-HOLE MOUNT	5012	Keystone
32	1	U1	InnoSwitch-3EP Switch Integrated Circuit, InSOP24D	INN3679C-H606	Power Integrations
33	1	VR1	DIODE ZENER 30V 500MW SOD123	MMSZ5256B-7-F	Diodes, Inc.

7 Transformer Specification

7.1 Electrical Diagram

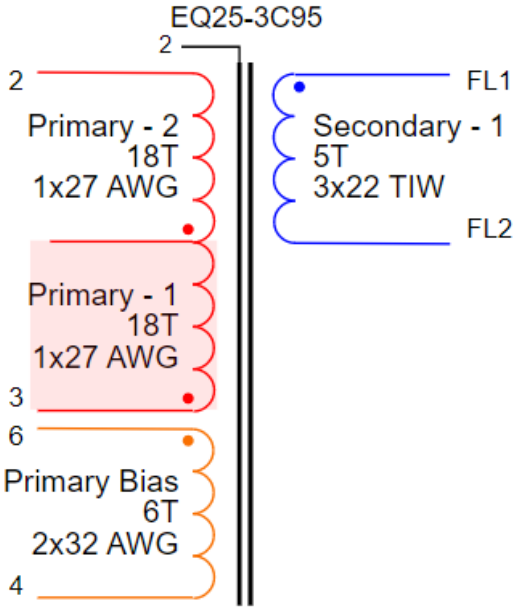


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Electrical Strength	60 second, 60 Hz, from pins 1, 2, 3, 4, 5, 6 to FL1 - FL2.	3000 VAC
Nominal Primary Inductance	Measured at 1 V_{PK-PK}, 100 kHz switching frequency, between pin 2 and 3, with all other windings open.	605 µH ±5%
Resonant Frequency	Between pin 2 and 3, other windings open.	1,000 kHz (Min.)
Primary Leakage Inductance	Between pin 2 and 3, with pins: 4, 6, FL1, FL2 shorted.	4.73 µH (Max.)

7.3 Material List

Item	Description
[1]	Core: EQ25, Ferroxcube: 3C95.
[2]	Bobbin: EQ25-Vert-6pins (6/0); PI#: 25-01136-00.
[3]	Magnet Wire: #27 AWG, Double Coated.
[4]	Magnet Wire: #32 AWG, Double Coated.
[5]	Magnet Wire: #22 AWG, Triple Insulated Wire.
[6]	Bus wire: #26AWG, Alpha Wire, Tinned Copper.
[7]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 7.5 mm Width.
[8]	Tape: 3M 13450-F, Polyester Film, 1 mil Thickness, 33 mm x 58 mm.
[9]	Varnish: Dolph BC-359.

7.4 Transformer Build Diagram

WD4:2nd Primary	18T - #27 AWG
WD3: Secondary	5T – 3 x #22 AWG
WD2: Bias	6T – 2 x 32 AWG
WD1: 1st Primary	18T - #27 AWG

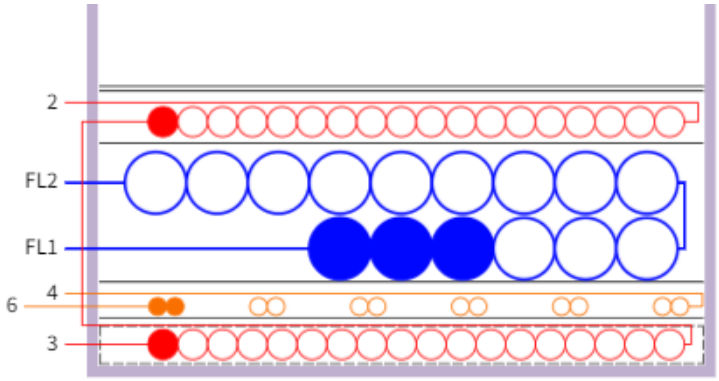


Figure 7 – Transformer Build Diagram.

7.5 Transformer Construction

Winding Preparation	Make slots with 2.0mm width on both flanges of secondary side of bobbin Item [2]. Position the bobbin Item [2] on the mandrel such that the primary side of the bobbin is on the left side. Winding direction is clock-wise direction for forward direction.
WD1 1st Primary	Start at pin 3, wind 18 turns of wire Item [3] in 1 layer, with tight tension, from left to right. At the last turn, leave the wire floating and enough length for WD4-2nd Primary.
Insulation	1 layer of tape Item [7].
WD2: Bias	Use 2 wires of Item [4] and wind 6 turns starting at pin 6 for bias winding. Spread the winding evenly across the entire bobbin. Finish this winding on Pin 4.
Insulation	1 layer of tape Item [7].
WD3 Secondary	Start at left slot of secondary side, use 3 wires Item [5], leaving ~ 40.0mm, and mark as FL1. Wind 5 tri-filar turns in 2 layers, from left to right, at the last turn exit the wires at right slot, also leaving ~ 30.0mm and mark FL2.
Insulation	1 layer of tape Item [7].
WD4 2nd Primary	Use floating wire from WD1-1st Primary, wind 18 turns from right to left and finish at pin 2.
Insulation	2 layer of tape Item [7].
Finish	Bring 3 wires marked as FL1 to the right and secure with 2 layers of tape Item [7]. Gap core halves to get 605 uH. Solder pin 4 with bus-wire Item [6] then lean along core halves and secure with tape. Varnish with Item [9]. Place 2 layers of tape Item [8] at the bottom then wrap up to the body of transformer, and tape around 1layer of tape Item [7].

8 Transformer Design Spreadsheet

1	ACDC_InnoSwitch3-EP_Flyback_030223; Rev.2.00; Copyright Power Integrations 2023	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3 EP Flyback Design Spreadsheet
2	**APPLICATION VARIABLES**					
3	VIN_MIN	63		63	V	Minimum AC input voltage
4	VIN_MAX	106		106	V	Maximum AC input voltage
5	VIN_RANGE			UNIVERSAL		Range of AC input voltage
6	LINEFREQ			60	Hz	AC Input voltage frequency
7	CAP_INPUT	100		100	uF	Input capacitor
8	VOUT	12.00		12.00	V	Output voltage at the board
9	CDC			0.00	mV	Cable drop compensation desired at full load
10	IOUT	4.160		4.160	A	Output current
11	POUT			49.92	W	Output power
12	EFFICIENCY			0.89		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
13	FACTOR_Z			0.50		Z-factor estimate
14	ENCLOSURE	OPEN FRAME		OPEN FRAME		Power supply enclosure
18	**PRIMARY CONTROLLER SELECTION**					
19	ILIMIT_MODE	STANDARD		STANDARD		Device current limit mode
20	DEVICE_GENERIC	INN36X9		INN36X9		Generic device code
21	DEVICE_CODE			INN3679C		Actual device code
22	POUT_MAX			75	W	Power capability of the device based on thermal performance
23	RDSON_100DEG			0.62	Ω	Primary switch on time drain resistance at 100 degC
24	ILIMIT_MIN			1.767	A	Minimum current limit of the primary switch
25	ILIMIT_TYP			1.900	A	Typical current limit of the primary switch
26	ILIMIT_MAX			2.033	A	Maximum current limit of the primary switch
27	VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
28	VDRAIN_ON_PRSW			0.37	V	Primary switch on time drain voltage
29	VDRAIN_OFF_PRSW			303.5	V	Peak drain voltage on the primary switch during turn-off
33	**WORST CASE ELECTRICAL PARAMETERS**					
34	FSWITCHING_MAX	76000		76000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
35	VOR	85.0		85.0	V	Secondary voltage reflected to the primary when the primary switch turns off
36	VMIN	90.00	Info	90.00	V	A manual overwrite of VMIN voids the value of input capacitor calculated by the tool or manually entered by the user and will be used for all calculations
37	KP			0.57		Measure of continuous/discontinuous mode of operation
38	MODE_OPERATION			CCM		Mode of operation
39	DUTYCYCLE			0.487		Primary switch duty cycle
40	TIME_ON			12.30	us	Primary switch on-time
41	TIME_OFF			6.75	us	Primary switch off-time
42	LPRIMARY_MIN			574.9	uH	Minimum primary inductance
43	LPRIMARY_TYP			605.2	uH	Typical primary inductance
44	LPRIMARY_TOL			5.0	%	Primary inductance tolerance
45	LPRIMARY_MAX			635.4	uH	Maximum primary inductance
47	**PRIMARY CURRENT**					
48	IPEAK_PRIMARY			1.885	A	Primary switch peak current
49	IPEDESTAL_PRIMARY			0.731	A	Primary switch current pedestal
50	IAVG_PRIMARY			0.591	A	Primary switch average current
51	IRIPPLE_PRIMARY			1.340	A	Primary switch ripple current

52	IRMS_PRIMARY			0.890	A	Primary switch RMS current
53						
54	SECONDARY CURRENT					
55	IPEAK_SECONDARY			13.571	A	Secondary winding peak current
56	IPEDESTAL_SECONDARY			5.266	A	Secondary winding current pedestal
57	IRMS_SECONDARY			6.577	A	Secondary winding RMS current
61	**TRANSFORMER CONSTRUCTION PARAMETERS**					
62	**CORE SELECTION**					
63	CORE	EQ25		EQ25		Core selection
64	CORE CODE			EQ25-3C95		Core code
65	AE			100.00	mm^2	Core cross sectional area
66	LE			41.40	mm	Core magnetic path length
67	AL			5710	nH/turns ^2	Ungapped core effective inductance
68	VE			4145.0	mm^3	Core volume
69	BOBBIN			EQ25 - 1 (P4-S0)		Bobbin
70	AW			39.69	mm^2	Window area of the bobbin - only the bobbin width and height are used to assess fit by the magnetics builder
71	BW			8.10	mm	Bobbin width
72	BH			4.90	mm	Bobbin height
73	MARGIN			0.0	mm	Safety margin width (Half the primary to secondary creepage distance)
75	**PRIMARY WINDING**					
76	NPRIMARY			36		Primary turns
77	BPEAK			3673	Gauss	Peak flux density
78	BMAX			3286	Gauss	Maximum flux density
79	BAC			1142	Gauss	AC flux density (0.5 x Peak to Peak)
80	ALG			467	nH/turns ^2	Typical gapped core effective inductance
88	**SECONDARY WINDING**					
89	NSECONDARY			5		Secondary turns
95	**BIAS WINDING**					
96	NBIAS			6		Bias turns
100	**PRIMARY COMPONENTS SELECTION**					
101	**LINE UNDERVOLTAGE**					
102	BROWN-IN REQURED			50.4	V	Required AC RMS line voltage brown-in range
103	RLS			2.60	MΩ	Connect two 1.3 MOhm resistors to the V-pin for the required UV/OV threshold
104	BROWN-IN ACTUAL			42.2 - 51.0	V	Actual AC RMS brown-in range
105	BROWN-OUT ACTUAL			36.0 - 43.0	V	Actual AC RMS brown-out range
107	**LINE OVERVOLTAGE**					
108	OVERVOLTAGE_LINE			194.4 - 220.6	V	Actual AC RMS line over-voltage range
109						
110	BIAS DIODE					
111	VBIAS			12.0	V	Rectified bias voltage
112	VF_BIAS			0.70	V	Bias winding diode forward drop
113	VREVERSE_BIASDIODE			36.75	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
114	CBIAS			22	uF	Bias winding rectification capacitor
115	CBPP			0.47	uF	BPP pin capacitor
119	**SECONDARY COMPONENTS**					
120	RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
121	RFB_LOWER			11.80	kΩ	Lower feedback resistor
122	CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor

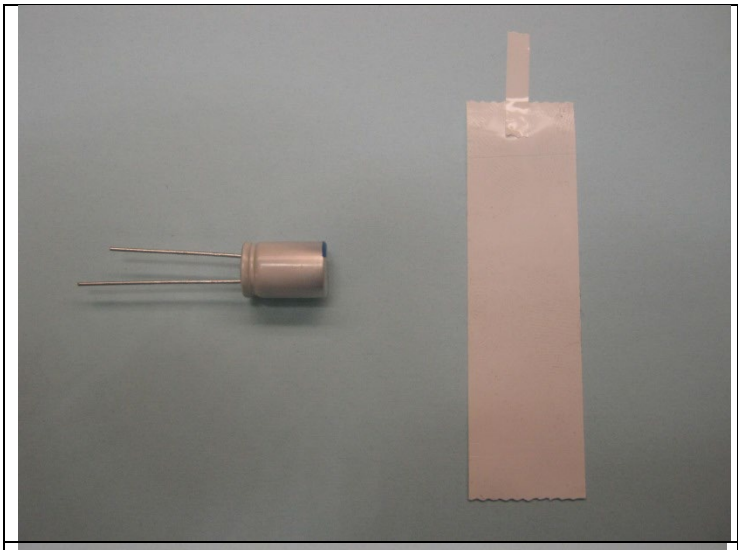
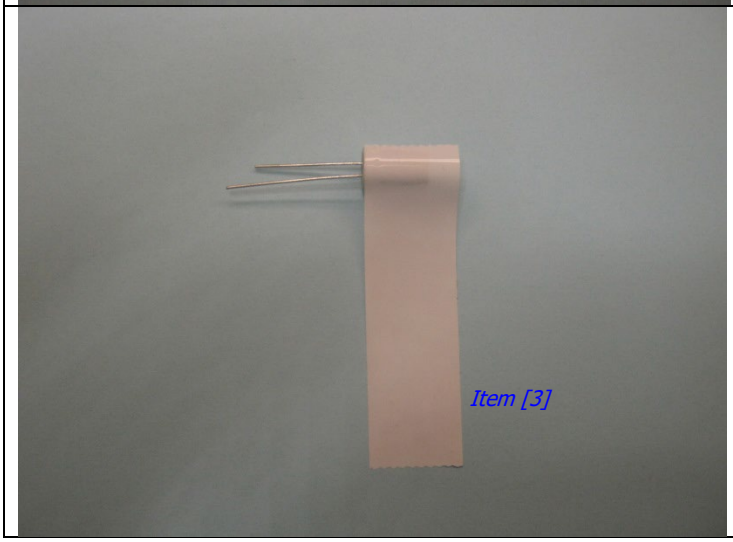
126	**MULTIPLE OUTPUT PARAMETERS**					
127	OUTPUT 1					
128	VOUT1			12.00	V	Output 1 voltage
129	IOUT1			4.16	A	Output 1 current
130	POUT1			49.92	W	Output 1 power
131	IRMS_SECONDARY1			6.577	A	Root mean squared value of the secondary current for output 1
137	NSECONDARY1			5		Number of turns for output 1
138	VREVERSE_RECTIFIER 1			32.63	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
139	SRFET1	AUTO		GKI06109		Secondary rectifier (Logic MOSFET) for output 1
140	VF_SRFET1			0.054	V	SRFET on-time drain voltage for output 1
141	VBREAKDOWN_SRFET 1			60	V	SRFET breakdown voltage for output 1
142	RDSON_SRFET1			13.1	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
144	**OUTPUT 2**					
145	VOUT2			0.00	V	Output 2 voltage
146	IOUT2			0.000	A	Output 2 current
147	POUT2			0.00	W	Output 2 power
148	IRMS_SECONDARY2			0.000	A	Root mean squared value of the secondary current for output 2
154	**NSECONDARY2**			0		Number of turns for output 2
155	VREVERSE_RECTIFIER 2			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 2
156	SRFET2	AUTO		NA		Secondary rectifier (Logic MOSFET) for output 2
157	VF_SRFET2			NA	V	SRFET on-time drain voltage for output 2
158	VBREAKDOWN_SRFET 2			NA	V	SRFET breakdown voltage for output 2
159	RDSON_SRFET2			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 2
161	**OUTPUT 3**					
162	VOUT3			0.00	V	Output 3 voltage
163	IOUT3			0.000	A	Output 3 current
164	POUT3			0.00	W	Output 3 power
165	IRMS_SECONDARY3			0.000	A	Root mean squared value of the secondary current for output 3
171	NSECONDARY3			0		Number of turns for output 3
172	VREVERSE_RECTIFIER 3			0.00	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 3
173	SRFET3	AUTO		NA		Secondary rectifier (Logic MOSFET) for output 3
174	VF_SRFET3			NA	V	SRFET on-time drain voltage for output 3
175	VBREAKDOWN_SRFET 3			NA	V	SRFET breakdown voltage for output 3
176	RDSON_SRFET3			NA	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 3
177						
178	PO_TOTAL			49.92	W	Total power of all outputs
179	NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

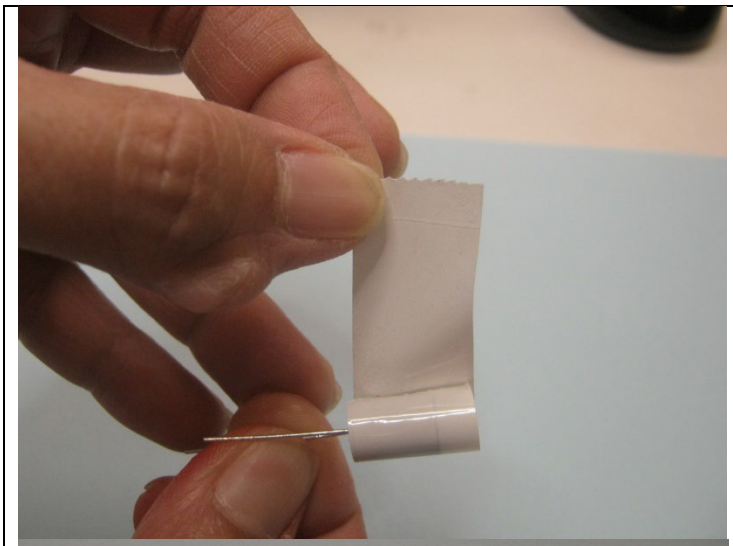
9 PCB Assembly Instructions

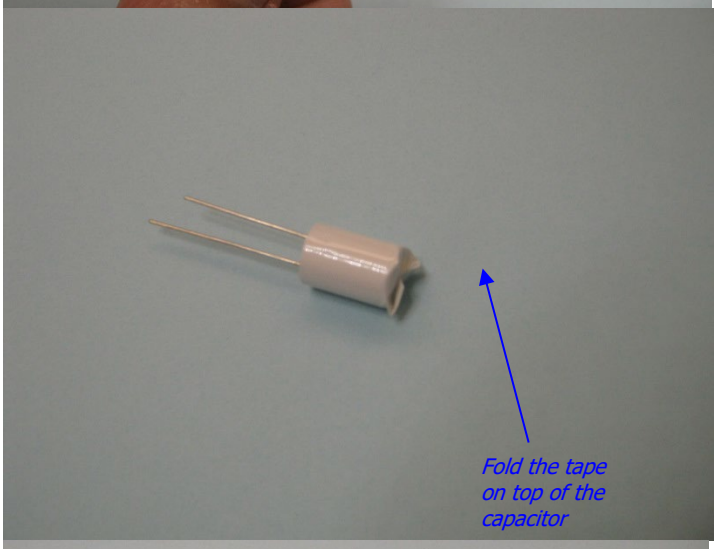
9.1 Materials

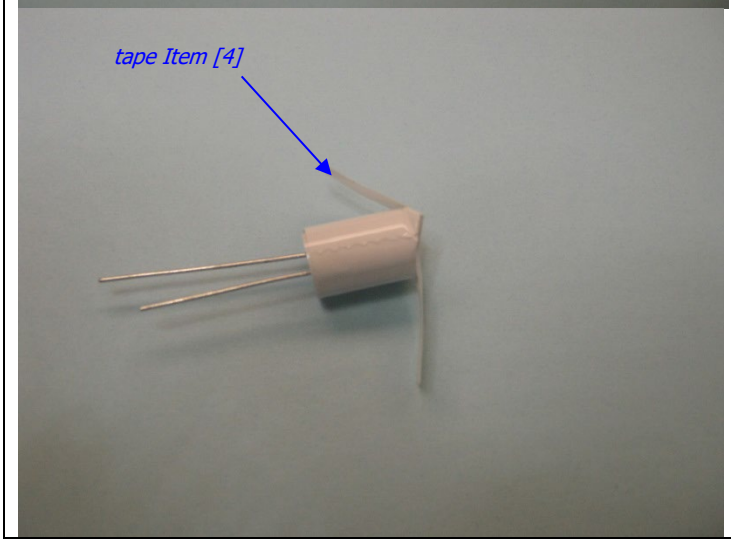
Item	Description
[1]	Capacitor C8 on RDR-747 Schematic.
[2]	Capacitor C9 on RDR-747 Schematic.
[3]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 16.4 mm Wide, 25 mm Long.
[4]	Tape: 3M 1298 Polyester Film, 1 mil Thick, 5.0 mm Wide, 15 mm Long.
[5]	Tape: 3M 4026W Double Coated Urethane Foam Tape 1.6 mm Thick, 12.7 mm Wide, 22 mm Long.

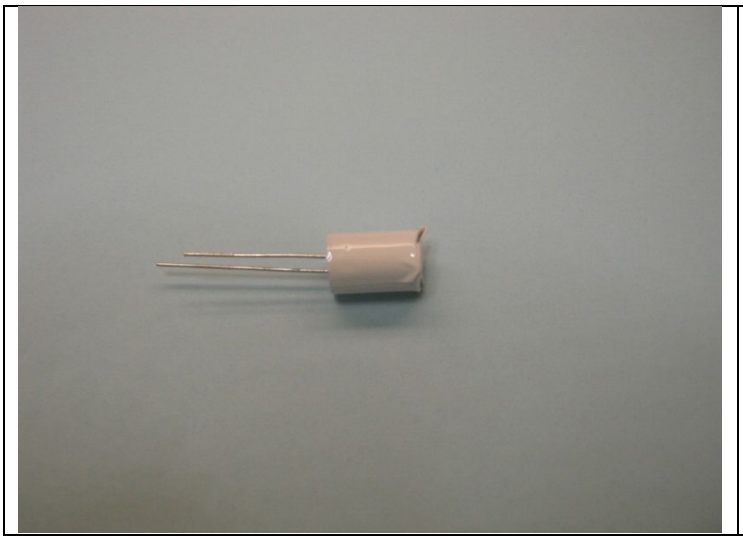
9.2 Output Capacitor Assembly Instructions

	
	Wrap C8 and C9 with tape Item [3] to insulate the capacitor form transformer core.




Fold the tape
on top of the
capacitor


tape Item [4]



Note: Cut all the TH (PTH and NPTH) pins to <0.5 mm on the bottom side of the board after completing the assembly.

10 Performance Data

All the performance data have been taken on the board unless otherwise specifically mentioned.

10.1 No-Load Input Power

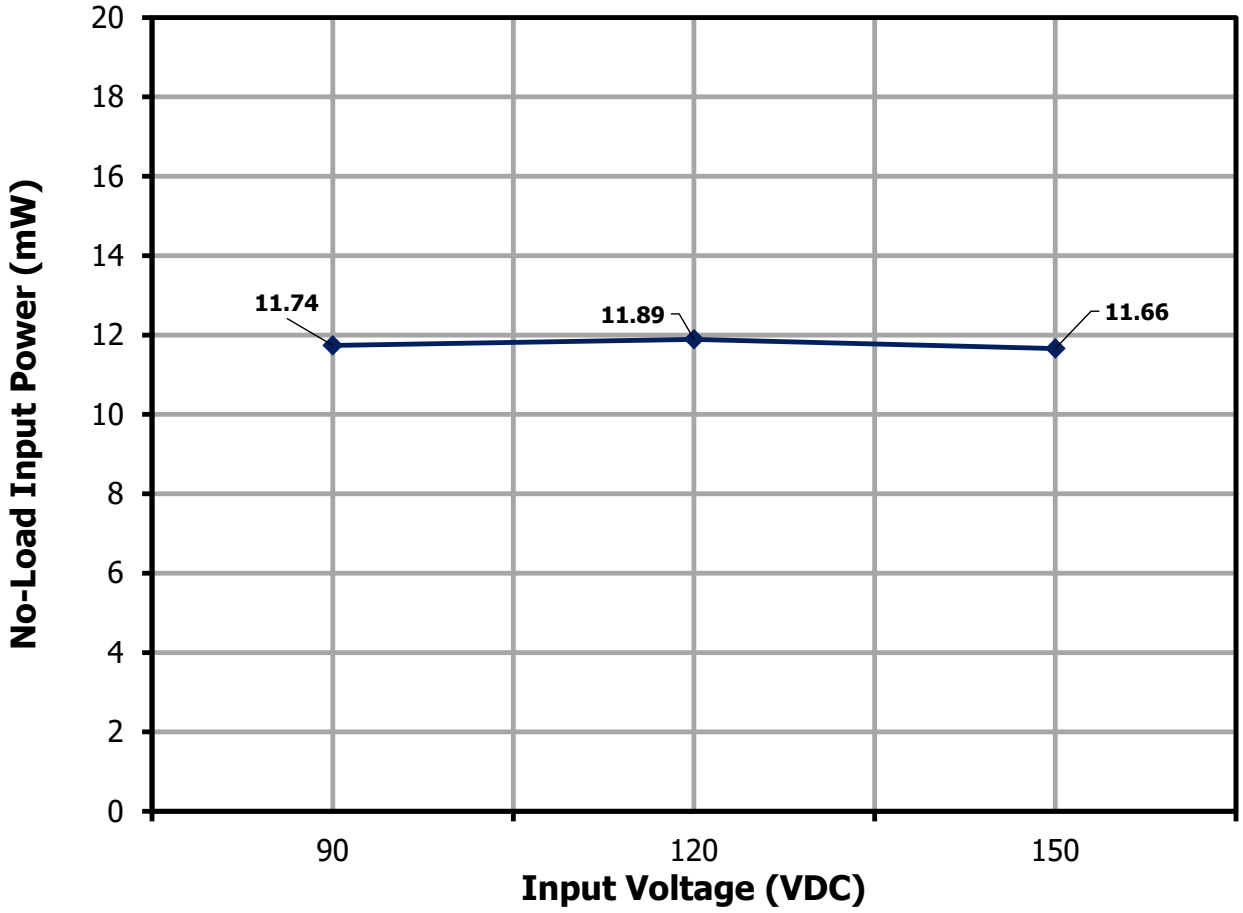


Figure 8 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

10.2 Efficiency

10.2.1 Line Efficiency

Line efficiency describes how the input voltage change affects the unit's overall efficiency. The points in the graph are only taken from 100% load conditions.

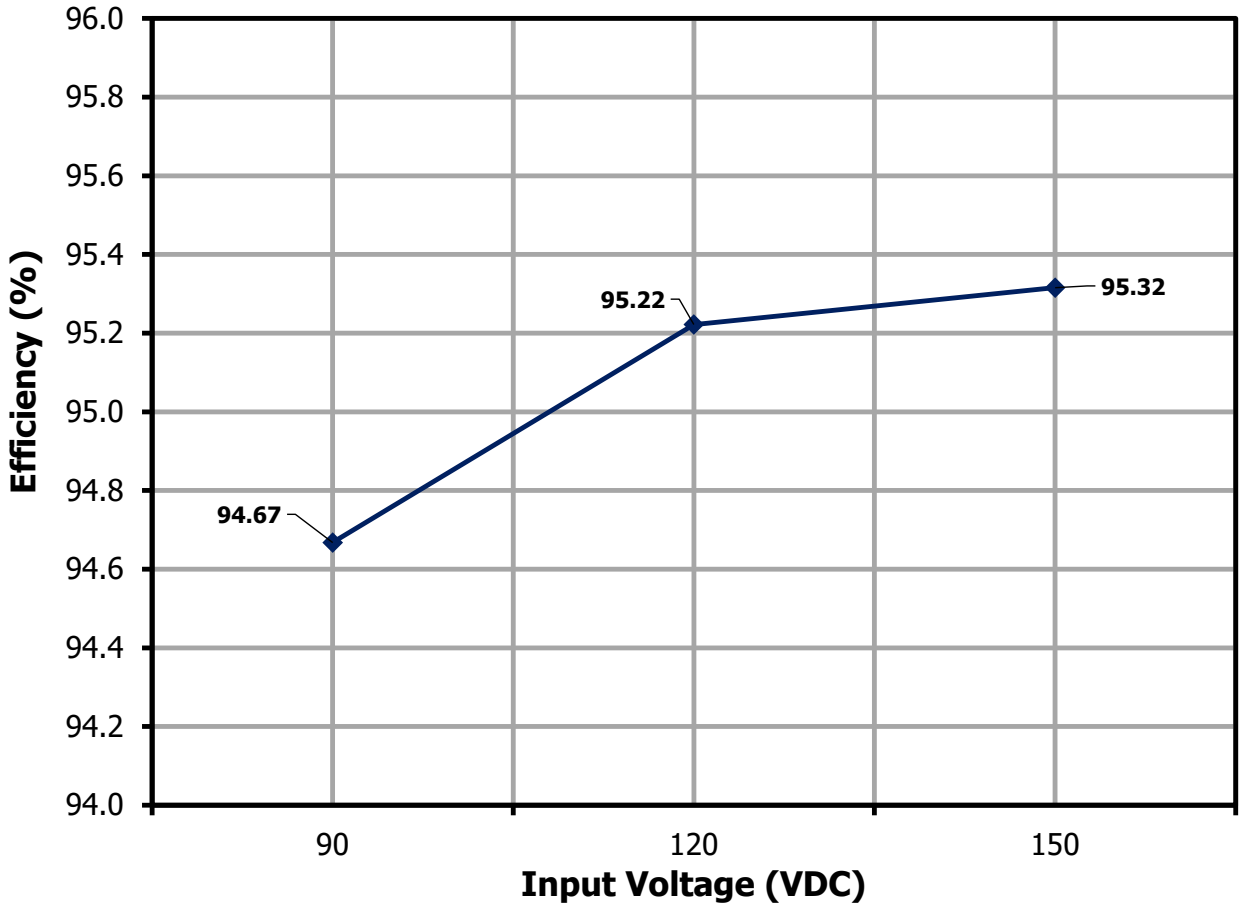


Figure 9 – Full-load Efficiency vs. Line, Room Ambient.

10.2.2 Load Efficiency

Load efficiency describes how the change in output loading conditions affects the unit's overall efficiency.

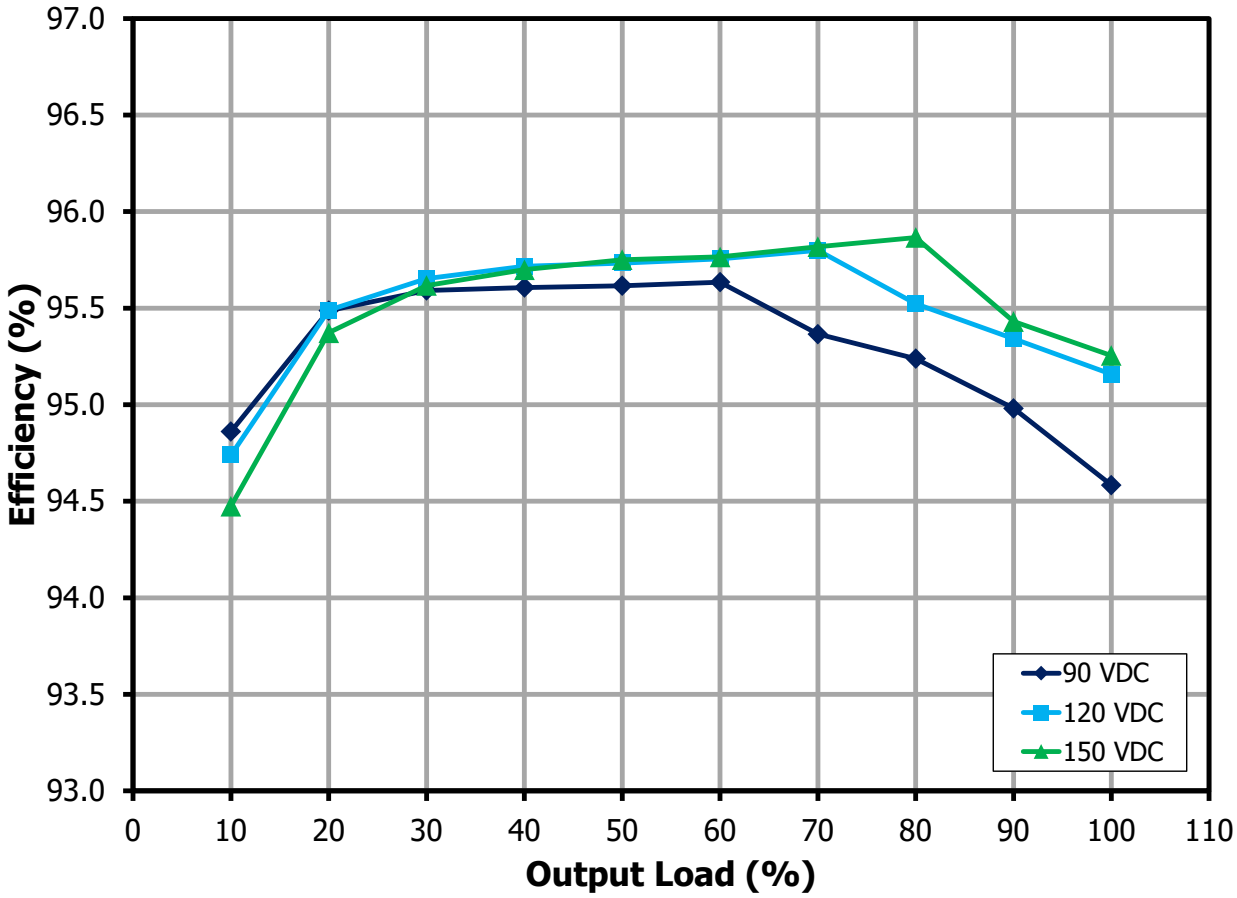


Figure 10 – Efficiency vs. Load at Different Input Voltages, Room Ambient.

10.3 Output Line and Load Regulation

10.3.1 Line Regulation

Line regulation describes how the change in input voltage conditions affects the average output voltage of the unit. The points in the following graph are only taken from 100% load conditions.

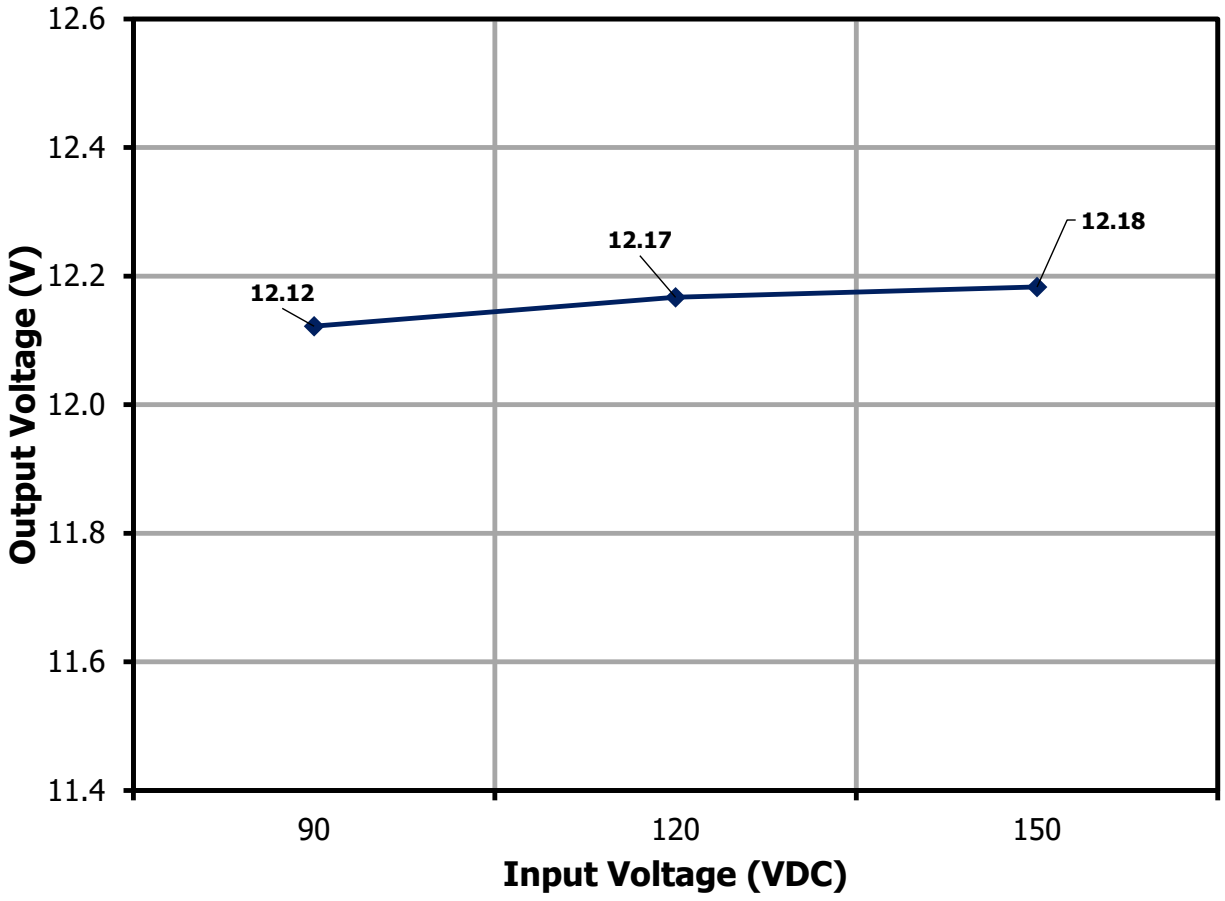


Figure 11 – Output Voltage vs. Input Voltage at Full Load, Room Temperature.

10.3.2 Load Regulation

Load Regulation describes how the change in output loading conditions affects the average output voltage of the unit.

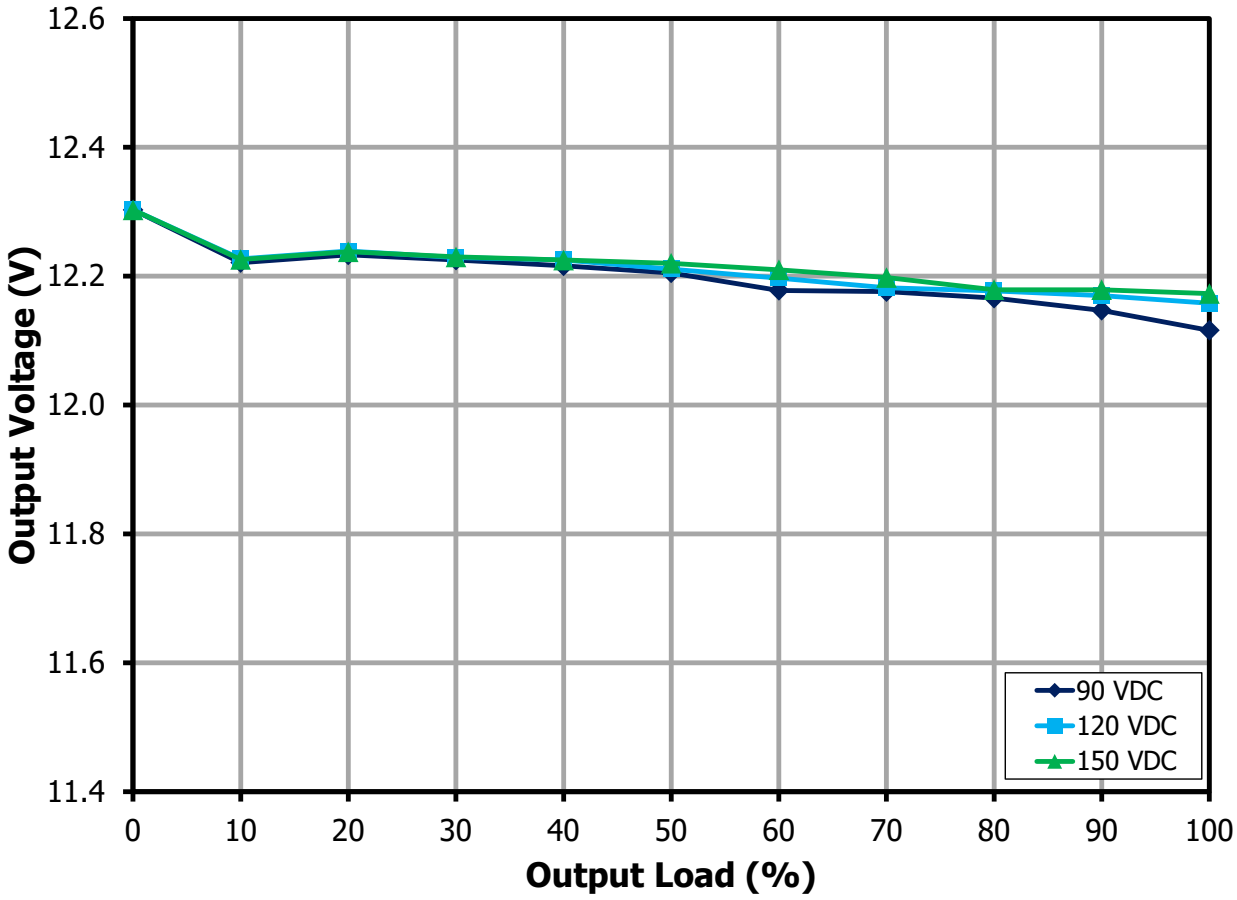


Figure 12 – Output Voltage vs. Load at Different Input Voltages, Room Temperature.

11 Thermal Performance

The following thermal scans are captured using a FLIR thermal imager after soaking for at least 1 hour. The set-up is inside an enclosure to minimize the effect of airflow.

11.1 90 VDC, 50 W at 20 ºC Ambient

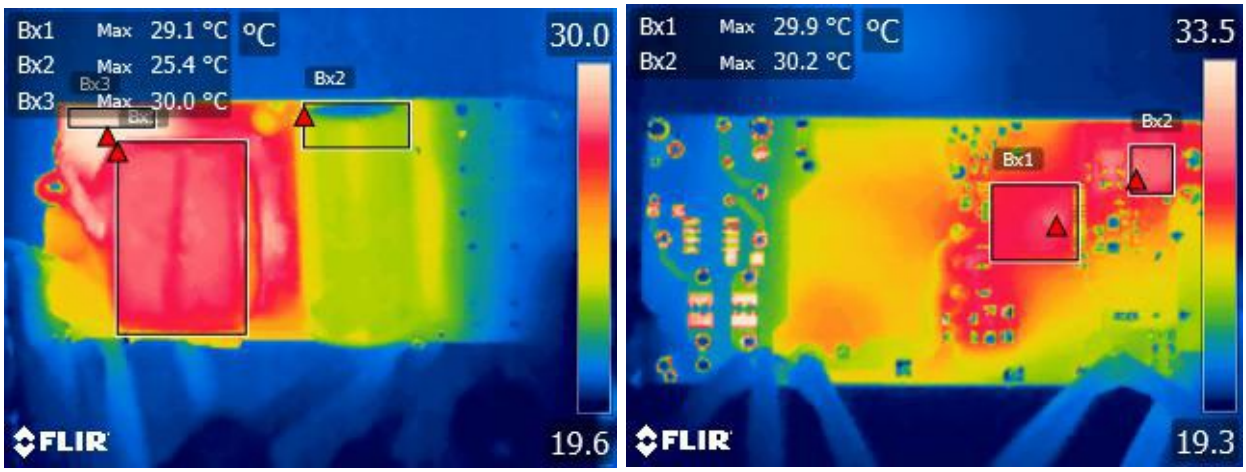


Figure 13 – Thermal Performance at 90 VDC Input.

Test condition setting: full load soaking up for 60 mins

Component	Transformer Winding (T1)	Input Capacitor (C2)	InnoSwitch3-EP (U1)	SR FET (Q1)
Max Temperature (ºC)	29.1	25.4	29.9	30.2

11.2 150 VDC Input, 50 W at 20 ºC Ambient

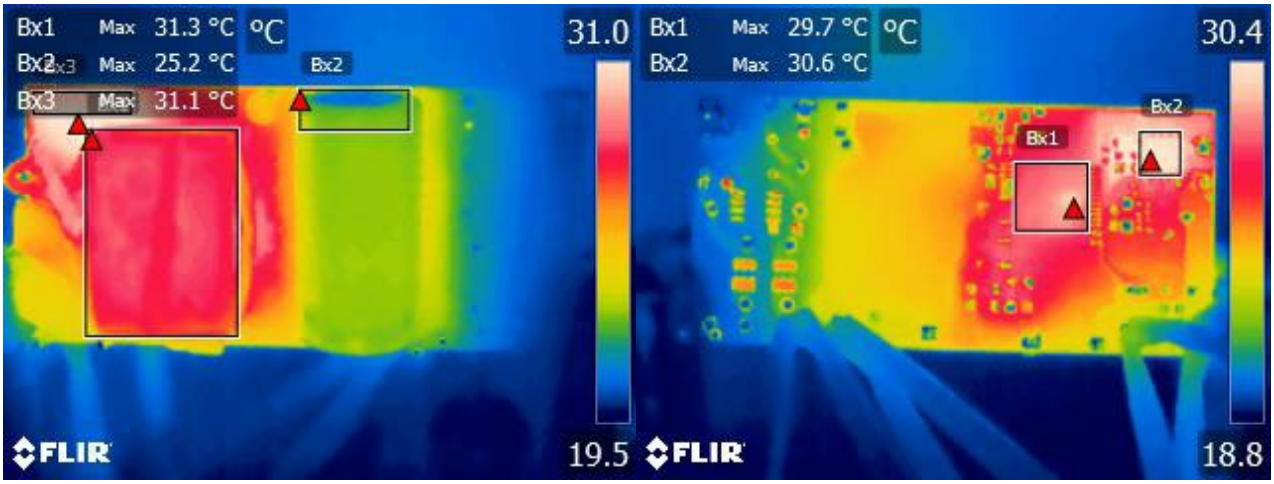


Figure 14 – Thermal Performance Over Time.

Test condition setting: full load soaking up for 60 mins

Component	Transformer Winding (T1)	Input Capacitor (C2)	InnoSwitch3-EP (U1)	SR FET (Q1)
Max Temperature (ºC)	31.3	25.2	29.7	30.6

12 Waveforms

12.1 Start-Up Waveforms

The following measurements were taken by connecting the unit under test at different test input voltages. An electronic load configured for constant current was used for all start-up tests.

12.1.1 Output Voltage and Current at 25 °C Ambient Temperature

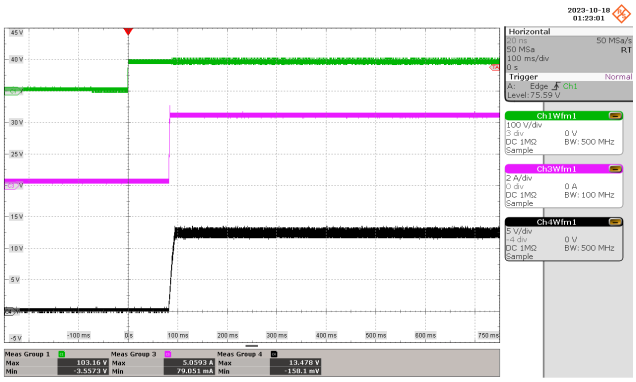


Figure 15 – Output Voltage and Current.
90 VDC, 100% Load.
CH1: V_{IN}, 100 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{OUT}, 5 V / div.
Time: 100 ms / div.

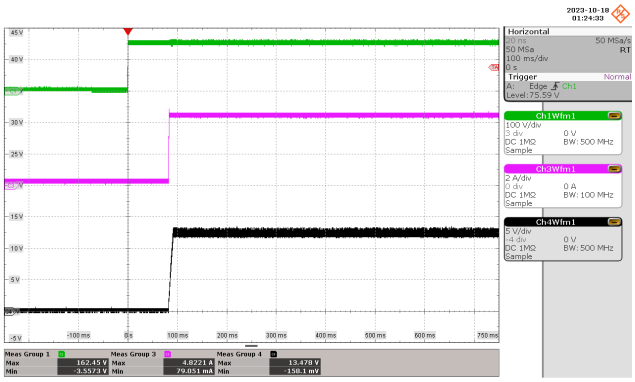


Figure 16 – Output Voltage and Current.
150 VDC, 100% Load.
CH1: V_{IN}, 100 V / div.
CH3: I_{OUT}, 2 A / div.
CH4: V_{OUT}, 5 V / div.
Time: 100 ms / div.

12.1.2 Innoswitch3-EP Drain Voltage and Current

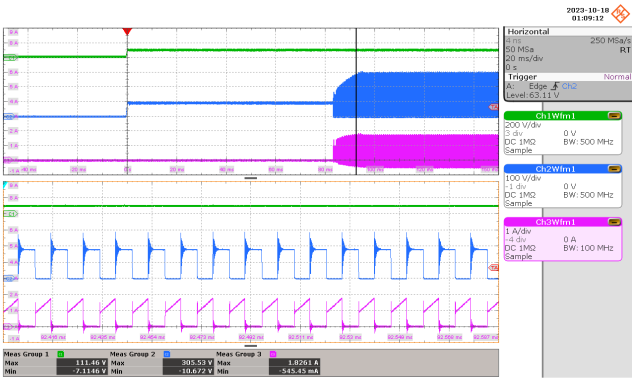


Figure 17 – Drain Voltage and Current Waveforms.
90 VDC, 100% Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{DS}, 100 V / div. (Max. 305.53 V)
CH3: I_{DS}, 1 A / div. (Max. 1.82 A)
Time: 20 ms / div.

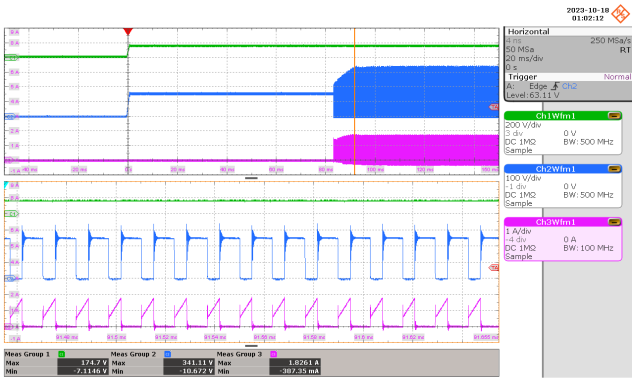


Figure 18 – Drain Voltage and Current Waveforms.
150 VDC, 100% Load.
CH1: V_{IN}, 200 V / div.
CH2: V_{DS}, 100 V / div. (Max. 341.11 V)
CH3: I_{DS}, 1 A / div. (Max. 1.82 A)
Time: 20 ms / div.

12.1.3 SR FET Drain Voltage and Current

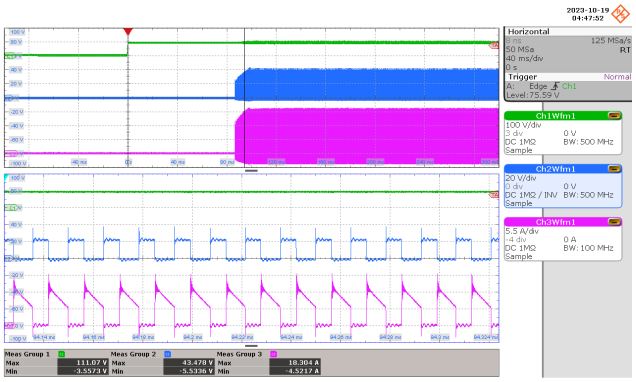


Figure 19 – Drain Voltage and Current Waveforms.
90 VDC, 100% Load.
CH1: VIN, 100 V / div.
CH2: VDS, 20 V / div. (Max. 46.64 V)
CH3: IDS, 3 A / div. (Max. 18.3 A)
Time: 20 ms / div.

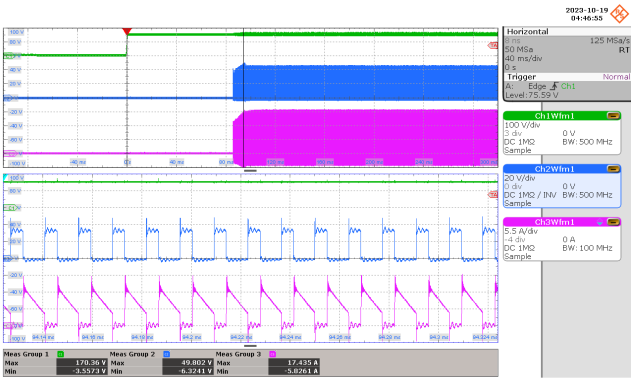


Figure 20 – Drain Voltage and Current Waveforms.
150 VDC, 100% Load.
CH1: VIN, 100 V / div.
CH2: VDS, 20 V / div. (Max. 51.38 V)
CH3: IDS, 3 A / div. (Max. 17.43 A)
Time: 20 ms / div.

12.2 Steady-State Waveforms

12.2.1 InnoSwitch3-EP Drain Voltage and Current at 25 °C Ambient Temperature

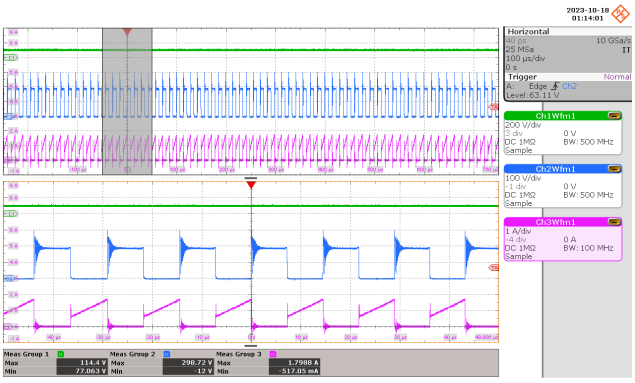


Figure 21 – Drain Voltage and Current Waveforms.
90 VDC, 100% Load.
CH1: Input, 200V / div.
CH2: V_{DRAIN}, 100 V / div. (Max. 298.72 V)
CH3: I_{DRAIN}, 1 A / div. (Max. 1.80 A)
Time: 200 μs / div.

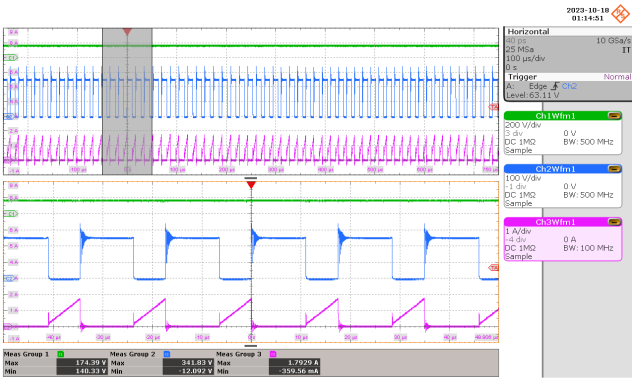


Figure 22 – Drain Voltage and Current Waveforms.
150 VDC, 100% Load.
CH1: Input, 200V / div.
CH2: V_{DRAIN}, 100 V / div. (Max. 341.83 V)
CH3: I_{DRAIN}, 1 A / div. (Max. 1.82 A)
Time: 200 μs / div.

12.2.2 SR FET Voltage

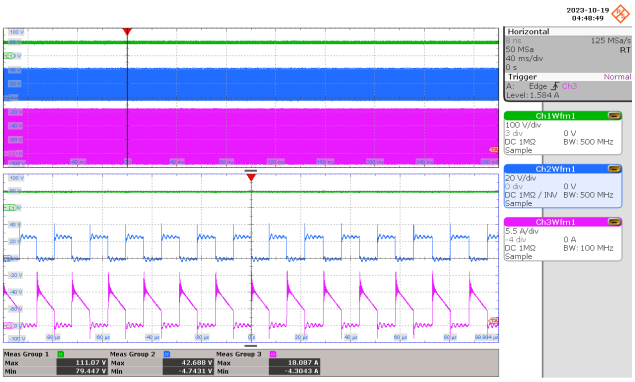


Figure 23 – SR FET Voltage Waveforms.
90 VDC, 100% Load.
CH1: Input, 200V / div.
CH2: V_{DRAIN}, 100 V / div. (Max. 43.47 V)
CH3: I_{DRAIN}, 1 A / div., (Max. 18.30 A)
Time: 20 ms / div.

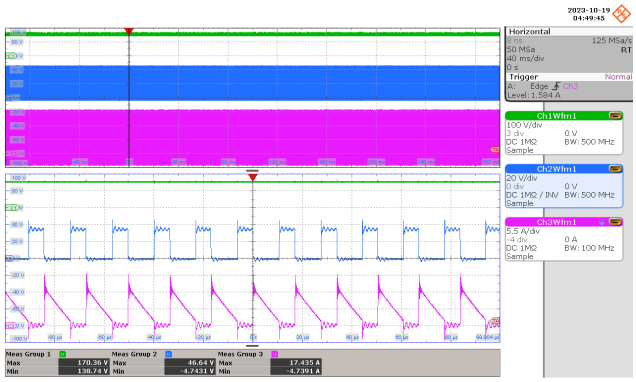


Figure 24 – SR FET Voltage Waveforms.
150 VDC, 100% Load.
CH1: Input, 200V / div.
CH2: V_{DRAIN}, 100 V / div. (Max. 46.64 V)
CH3: I_{DRAIN}, 1 A / div., (Max. 17.43 A)
Time: 20 ms / div.

12.3 Load Transient Response (On Board)

Output voltage waveform on the board was captured with dynamic load transient from 0% to 100%. The duration for the load states is set to 500 ms, and the load slew rate is 800 mA / µs. The test is done at 25 °C ambient temperature.

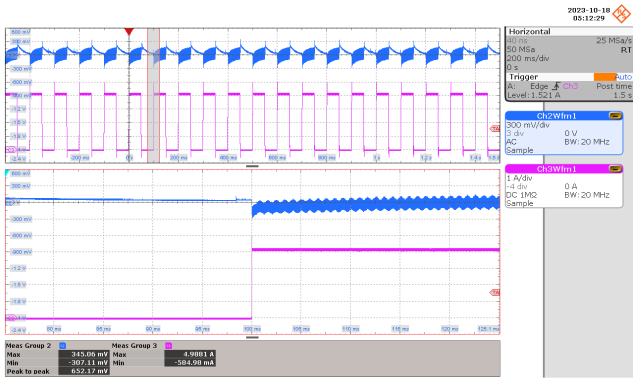


Figure 25 – Transient Response.
90 VDC, 0% – 100% Load Step.
ΔV-: -307 mV, ΔV+: 345 mV.
Upper: V_{OUT}, 300 mV / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.

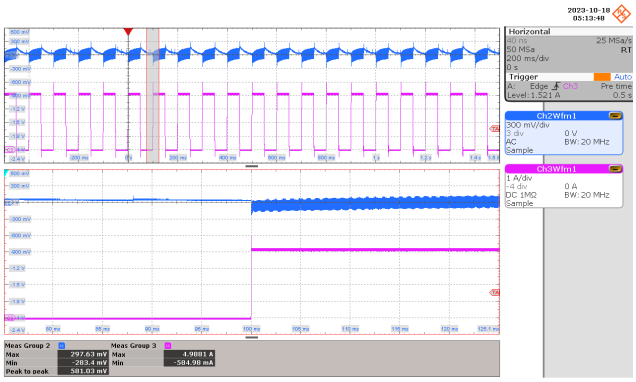


Figure 26 – Transient Response.
150 VDC, 0% – 100% Load Step.
ΔV-: -283 mV, ΔV+: 297 mV.
Upper: V_{OUT}, 300 mV / div., 5 ms / div.
Lower: I_{LOAD}, 1 A / div.

12.4 Output Ripple Measurements

12.4.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

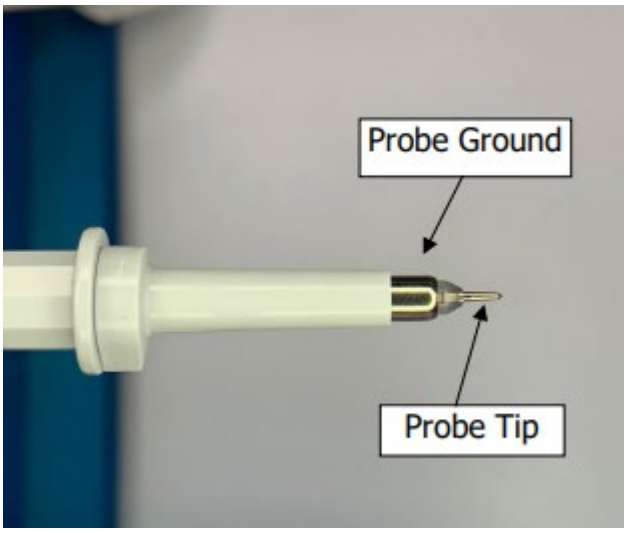


Figure 27 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

Figure 28 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

12.4.2 Ripple Amplitude vs. Load

12.4.2.1 Ripple Plot

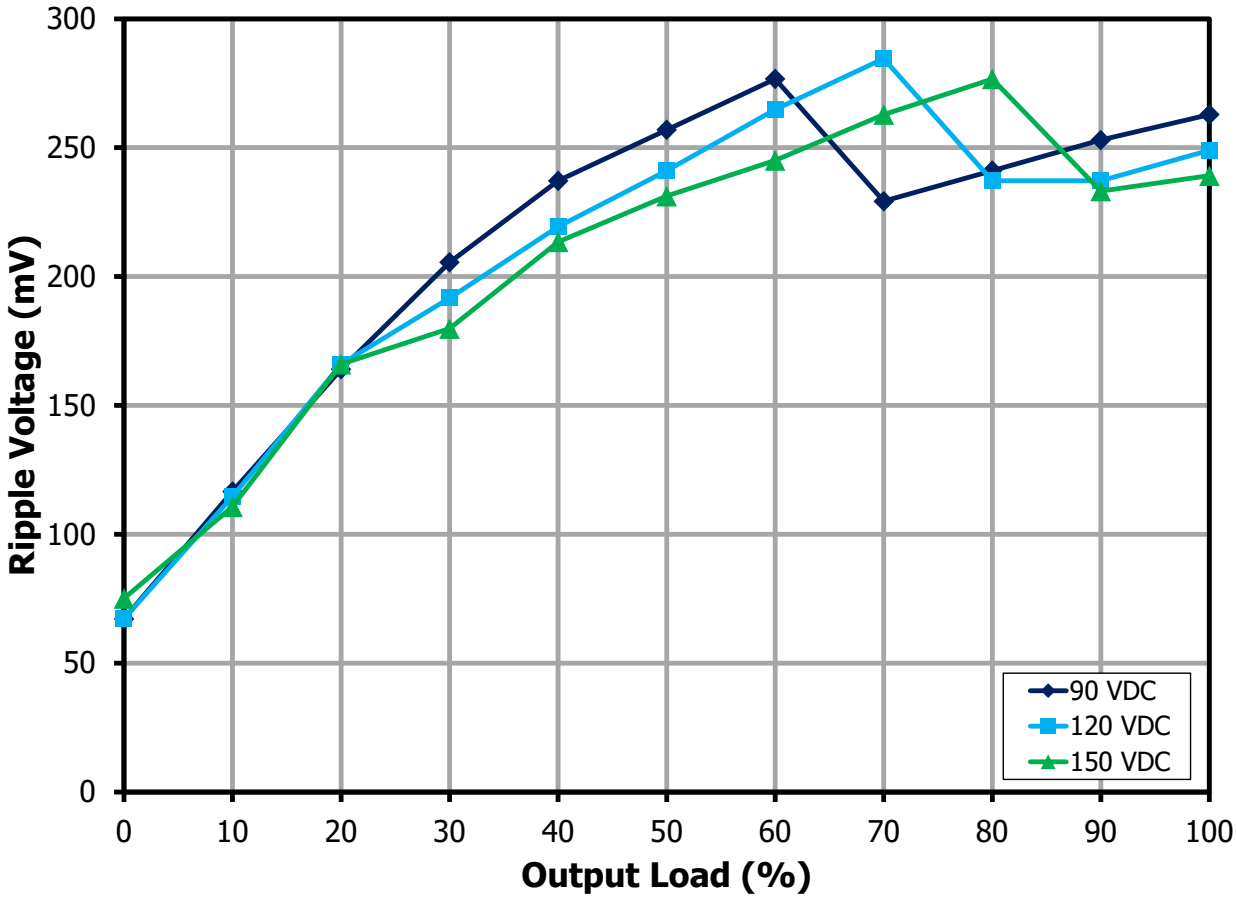


Figure 29 – Ripple Amplitude vs. Output Power, 12 V_{OUT}.

Input	90 VDC	120 VDC	150 VDC
Max Ripple (mV)	277	285	277

12.4.2.3 Ripple Waveforms

Output voltage ripple waveform was captured at the output terminals using the ripple measurement probe with a decoupling capacitor. The waveforms shown are taken at the load setting where the highest ripple was observed for every input voltage setting.

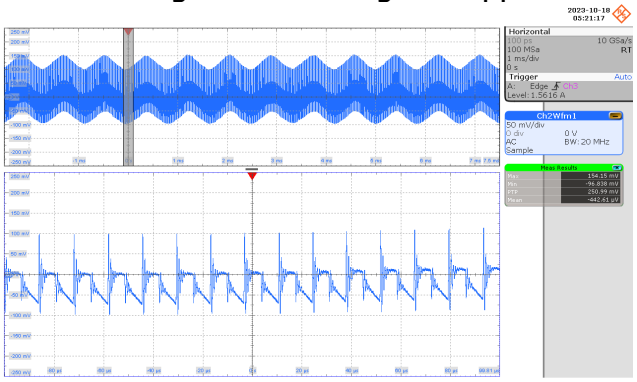


Figure 30 – Output Ripple. (PK-PK – 250 mV)
90 VDC Input, 100% Load.
V_{OUT}, 50 mV / div., 1 ms / div.

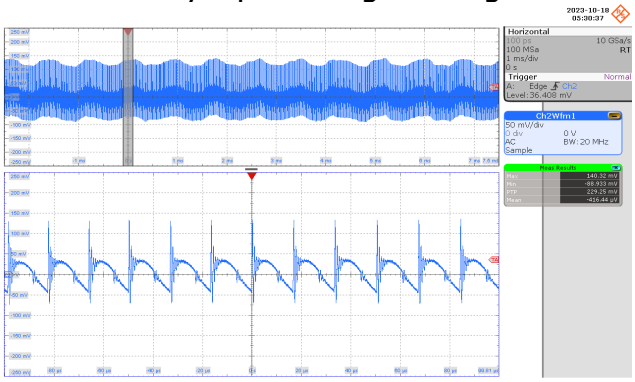


Figure 31 – Output Ripple. (PK-PK – 230 mV)
150 VDC Input, 100% Load.
V_{OUT}, 50 mV / div., 1 ms / div.

12.5 Short-Circuit Protection

The unit was tested by applying an output short-circuit during start up and normal working conditions and then removing the short-circuit to see if the unit could recover and operate normally. The expected response during short-circuit is for the unit to go to AR (auto-restart) mode and attempt recovery every 1.7 to 2.11 seconds.

12.5.1 Start-up Short

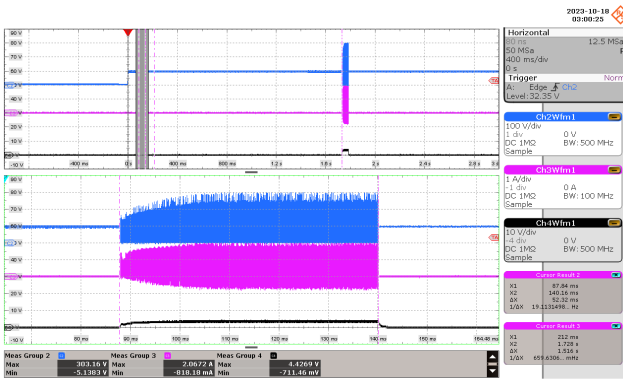


Figure 32 – INN3679C Drain Voltage and Current.
90 VDC, Output Short.
CH2: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 1 A / div., 10 µs / div.
CH4: Output, 10 V / div.
Time 2s / div.

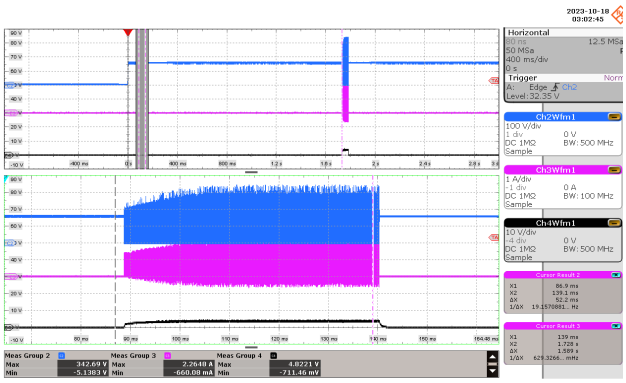


Figure 33 – INN3679C Drain Voltage and Current.
150 VDC, Output Short.
CH2: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 1 A / div., 10 µs / div.
CH4: Output, 10 V / div.
Time 2s / div.

12.5.2 Normal Operation to Short

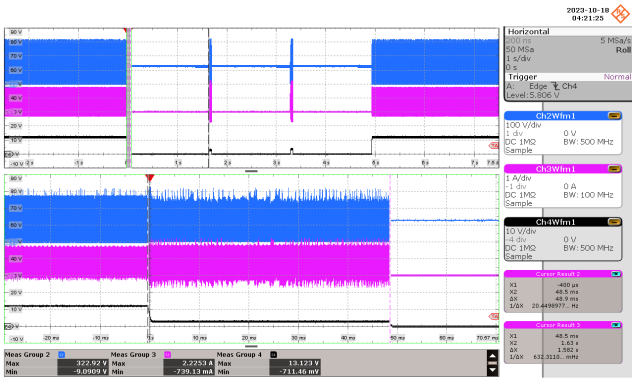


Figure 34 – INN3679C Drain Voltage and Current 90 VDC, Output Short.
CH2: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 1 A / div., 10 µs / div.
CH4: Output, 10 V / div.
Time 2s / div.

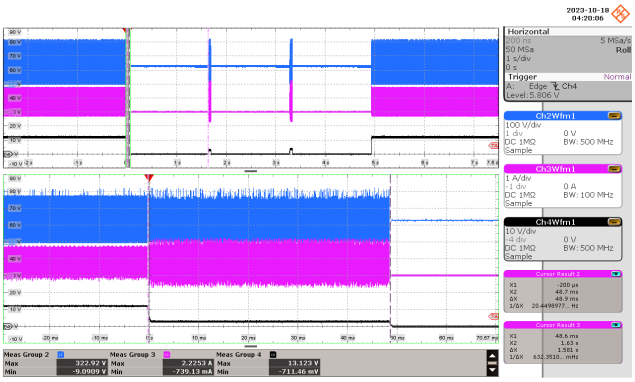


Figure 35 – INN3679C Drain Voltage and Current 150 VDC, Output Short.
CH2: V_{DRAIN}, 100 V / div.
CH3: I_{DRAIN}, 1 A / div., 10 µs / div.
CH4: Output, 10 V / div.
Time 2s / div.

13 Revision History

Date	Author	Revision	Description & Changes	Reviewed
19-Oct-23	AMC	1.0	Initial Release.	Apps & Mktg

For the latest updates, visit our website: www.power.com

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