Design Example Report

Title	***9.9 W, Wide Range Input, Dual Output, Isolated Flyback Converter for Anti-Magnetizing Interference Using LinkSwitch™-XT2-900 LNK3696P***
Specification	85 VAC – 350 VAC Input; 18 V / 300 mA, 18 V / 250 mA Outputs
Application	Metering
Author	Applications Engineering Department
Document Number	DER-708
Date	December 20, 2021
Revision	1.0

Summary and Features

- Highly integrated solution with 900 V rated power MOSFET
- Output voltage regulation: 18 V ±5%, 18 V ±10%
- Programmable current limit selection feature of LinkSwitch-XT2-900
- >82% efficiency at full load condition, nominal input voltage
- <130 mW no-load input power at 230 VAC
- >6 dB conducted EMI margin
- Can operate up to 350 VAC line input
- Can withstand 6 kV differential line surge
- Can withstand external magnetizing interference

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

1 Introduction

This engineering report describes a dual output flyback converter that can provide an 18 V at 300 mA isolated output and 18 V at 250 mA non-isolated output from a wide input voltage range of 85 VAC to 350 VAC. It was designed to withstand external magnetizing interference for metering applications. This adapter utilizes the LNK3696P from the LinkSwitch-XT2 900 V family of devices.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

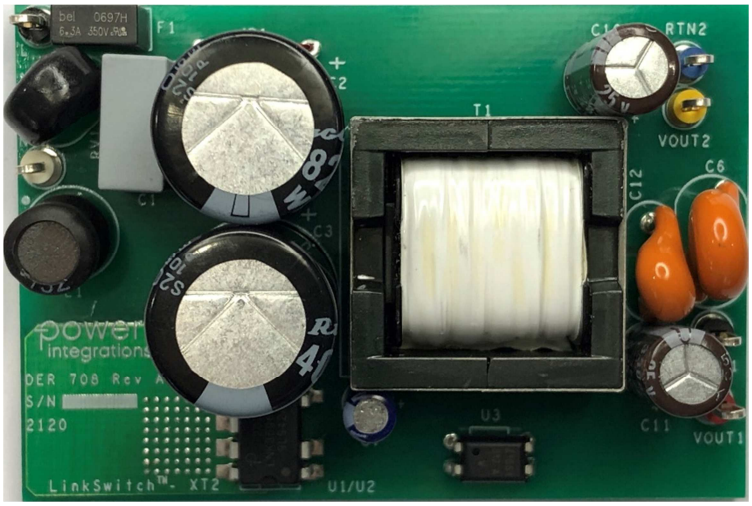


Figure 1 – Populated Circuit Board Photograph, Top.

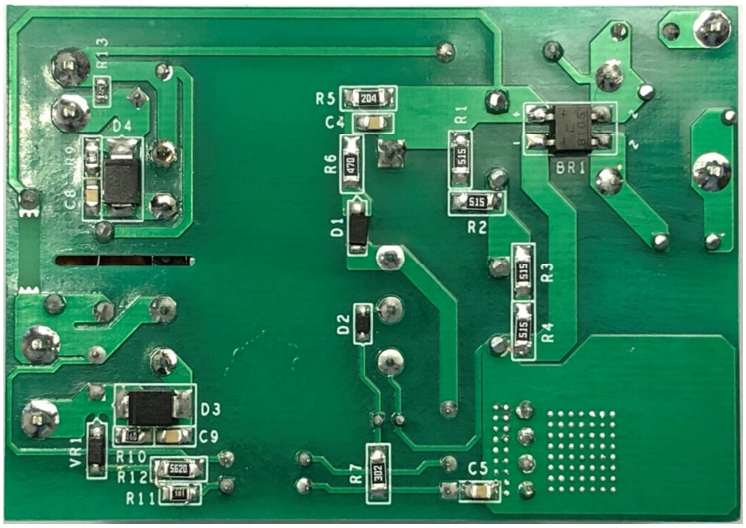


Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85	230	350	VAC	2 Wire – no P.E. Verified at 350 VAC.
Frequency	f_{LINE}	50	50/60	60	Hz	
No-load Input Power				150	mW	230 VAC.
Output						
Output Voltage 1	V_{OUT-1}	17.1	18	18.9	V	±5%
Output Current 1	I_{OUT-1}	30	300		mA	
Output Voltage 2	V_{OUT-2}	16.2	18	19.8	V	±10%
Output Current 2	I_{OUT-2}	25	250		mA	
Output Ripple Voltage	V_{RIPPLE}			240	mV	20 MHz Bandwidth.
Output Power	P_{OUT}		9.9		W	
Efficiency						
Full Load	$\eta_{Full-Load}$		82		%	At Nominal Input Voltage, Measured at Output Terminal.
Environmental						
Conducted EMI			CISPR22B / EN55022B Load floating			Resistive Load, 6 dB Margin.
Line Surge						
Differential Mode (L/N)				6	kV	Differential: 2 Ω
Ambient Temperature	T_{AMB}	0		50	°C	Free Convection, Sea Level in Sealed Enclosure.

3 Schematic

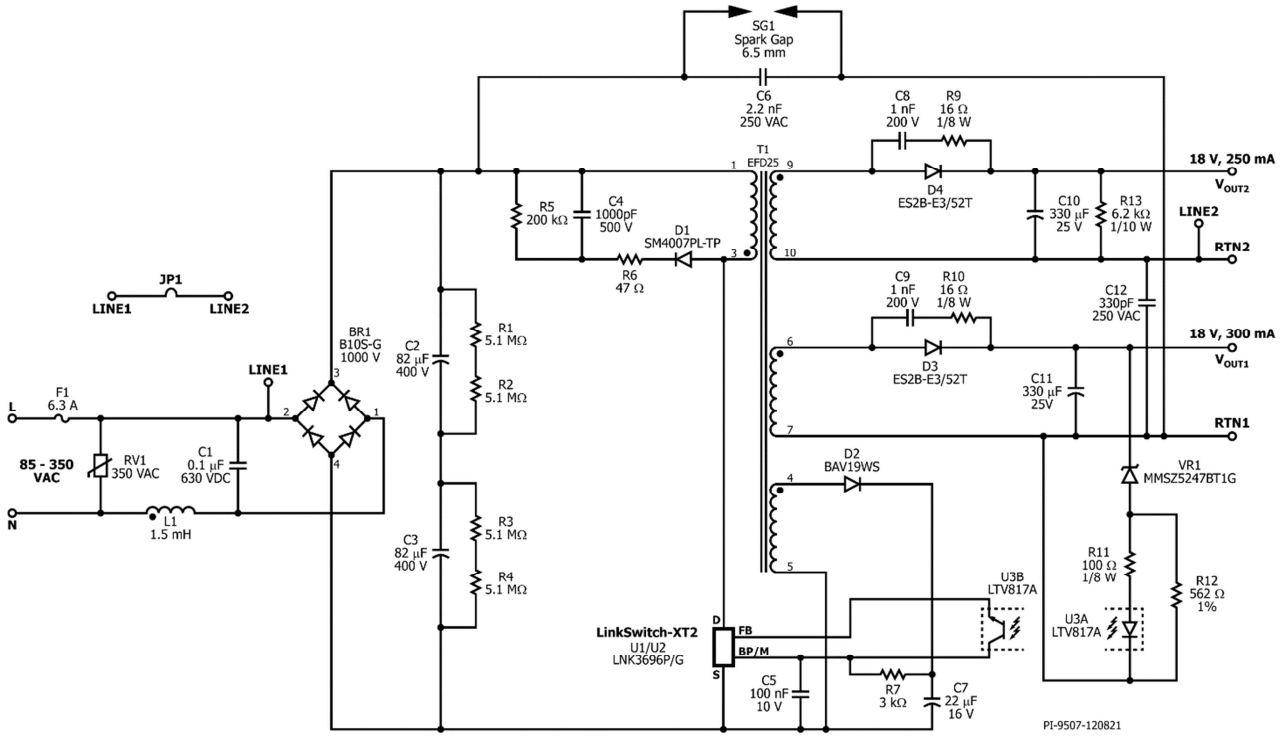


Figure 3 – Schematic.

4 Circuit Description

The LinkSwitch-XT2 900 V family of devices integrates a high-voltage (900 V rated) power MOSFET with an internal oscillator and ON/OFF controller inside a single monolithic IC. Unlike conventional pulse width modulation (PWM) controllers, LinkSwitch-XT2 900 V devices utilize a simple ON/OFF control scheme combined with an internal current limit circuitry to regulate the output voltage. The LNK3696P IC was used in a flyback converter with dual output (18 V isolated and 18 V non-isolated) delivering 300 mA and 250 mA respectively.

4.1 Input Rectifier and Filter

Fuse F1 isolates the circuit and provides protection from component failure. The AC input is rectified by bridge rectifier BR1 and filtered by the bulk storage capacitors C2 and C3. Filter formed by C1, C2, C3, and L1, form a differential mode noise attenuator. Resistors R1, R2, R3 and R4 function to balance the voltage between the bulk capacitors in series. Varistor RV1 is used to clamp the voltage during line surge events.

4.2 LinkSwitch-XT2 Primary Side

The LNK3696P device (U1/U2) integrates the oscillator, controller, start-up and other protection circuitry as well as the high-voltage power MOSFET on a single monolithic IC.

The LNK3696P IC operates at a fixed current limit (I_{LIMIT}). Every enabled switching cycle, the primary current ramps to this current limit level. Output regulation is maintained by skipping switching cycles (ON/OFF control). The internal controller determines if the next switching cycle should be enabled or disabled (skipped) based on the current flowing into the FEEDBACK (FB) pin. If a current less than 49 μA flows into the FB pin when the oscillator's (internal) clock signal occurs, power MOSFET switching is enabled for that switching cycle and the power MOSFET turns on. If the current is greater than 49 μA then the power MOSFET is disabled for the current switching cycle.

The switching cycle terminates when the current through the power MOSFET reaches I_{LIMIT}, or the on-time of the power MOSFET reaches the maximum duty cycle (DC_{MAX}) limit.

At full load, few switching cycles will be skipped (disabled), resulting in a high effective switching frequency. As the load reduces, more switching cycles are skipped, which reduces the effective switching frequency. At no-load, most switching cycles are skipped, which is what makes the no-load power consumption of supplies designed around the LinkSwitch-XT2 family so low, since switching losses are the dominant loss mechanism at light loading. Additionally, since the amount of energy per switching cycle is fixed by I_{LIMIT}, the skipping of switching cycles gives the supply a flat efficiency characteristic over the load range.

4.3 Primary RCD Clamp

A low cost RCD clamp is connected across the primary winding of transformer T1. This is composed of resistors R5 and R6, capacitor C4 and diode D1. The clamp helps in dissipating the energy stored in the leakage inductance of T1.

4.4 Auxiliary Winding

The IC is self-starting, using an internal high-voltage current source to charge the BP pin capacitor (C5) when AC is first applied. During normal operation the primary side block is powered from an auxiliary winding on the transformer T1. Output of the auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C7. Resistor R7 limits the current being supplied to the BP pin of the LinkSwitch-XT2 (U1/U2).

4.5 Output Rectification

Transformer T1 has two secondary windings on its core – one for each output voltage. For both secondaries, the secondary switching voltage is rectified by ultrafast diodes D3 and D4, and then filtered by very low ESR type capacitors C10, and C11. For each ultrafast diode, a snubber network is connected in parallel using resistors R9 and R10, and capacitors C8 and C9. The snubber network helps limit the peak inverse voltage spikes seen by the diode. A pre-load resistor R13 is connected on the second 18 V output to improve minimum load regulation performance.

4.6 Output Feedback

The first (isolated) 18 V_{OUT1} output is sensed through the Zener diode-optocoupler network consisting of diode VR1, resistors R11 and R12, and optocoupler U3. The current through U3, which is set by resistors R11 and R12, is fed back to U1/U2 through the FEEDBACK (FB) pin. This current should be high enough for optimal feedback sensitivity and output regulation and should be low enough to minimize no-load input power. The second (non-isolated) 18 V_{OUT2} output is regulated through the coupling of the two output windings.

5 PCB Layout

Layers: Two (2)
Board Materials: FR4
Board Thickness: 1.59 mm
Copper weight: 2 oz

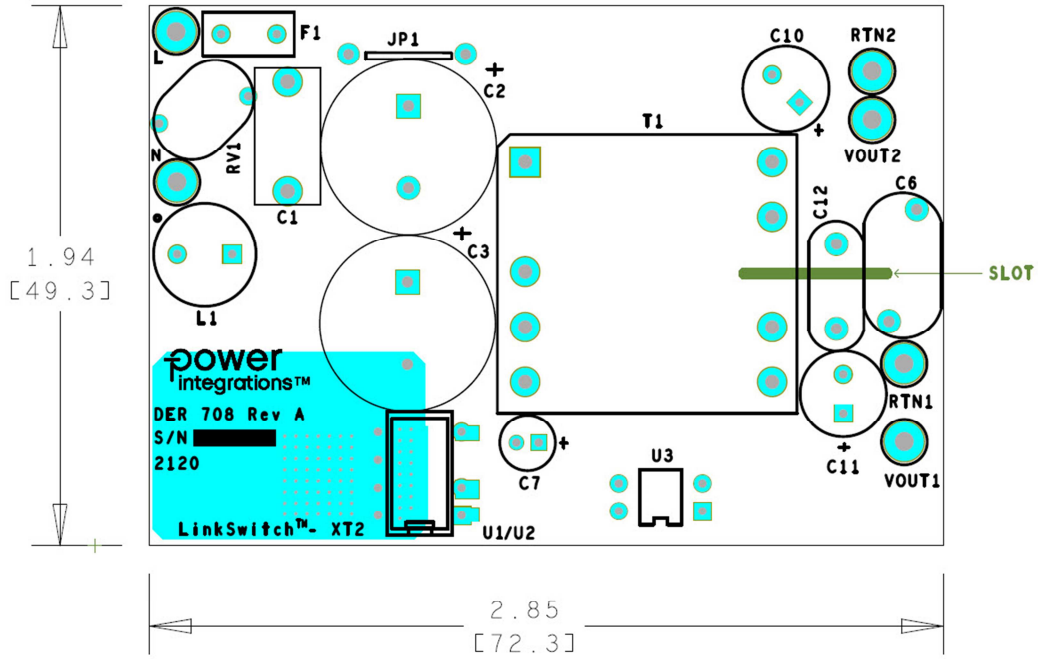


Figure 4 – Printed Circuit Layout, Top.

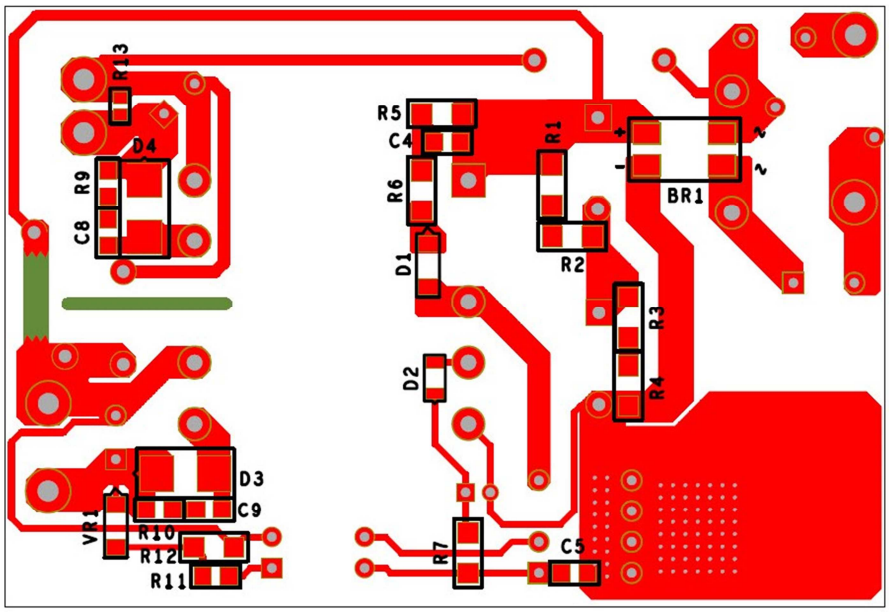


Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1	0.1 µF, ±20%, Film, X2 Safety Rated, 310 VAC, 630 VDC, Polypropylene (PP), Metallized Radial	BFC233920104	Vishay
3	2	C2, C3	82 µF, 400 V, General Purpose, Electrolytic, (16 x 25)	400LXW82MEFR16X25	Rubycon
4	1	C4	1000 pF, 10%, 500 V, Ceramic, X7R, 0805	C0805C102KCRACTU	Kemet
5	1	C5	100 nF, 0.1 uF, 10 V, Ceramic, X7R, 0805	0805ZC104MAT2A	AVX
6	1	C6	2200 PF, ±20%, 500 VAC (Y1),760 VAC (X1), Ceramic, Y5U (E), RADIAL	440LD22-R	Vishay
7	1	C7	22 µF, 16 V, Electrolytic, Gen. Purpose, (5 x 11)	ECA-1CM220	Panasonic
8	2	C8, C9	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	2	C10, C11	330 µF, 25 V, Electrolytic, Very Low ESR, 56 m Ω, (8 x 15)	EKZE250ELL331MH15D	Nippon Chemi-Con
10	1	C12	330 pF, Ceramic Y1	440LT33-R	Vishay
11	1	D1	1000 V, 1 A, Standard Recovery, SOD-123FL	SM4007PL-TP	Micro Commercial
12	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
13	2	D3, D4	100 V, 2 A, Ultrafast Recovery, 20 ns, DO-214AA	ES2B-E3/52T	General Semi
14	1	F1	FUSE BRD MNT 6.3 A 350 VAC 72 VDC	0697H6300-02	Belfuse
15	1	L1	INDUCTOR, FIXED, 1.5 mH, 430 mA, 3.8 Ω, TH	RLB9012-152KL	Bourns
16	4	R1, R2, R3, R4	RES, 5.1 MΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ515V	Panasonic
17	1	R5	RES, 200 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ204V	Panasonic
18	1	R6	RES, 47 Ω, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ470V	Panasonic
19	1	R7	RES, 3.0 kΩ, 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ302V	Panasonic
20	2	R9 R10	RES, 16 Ω, 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ160V	Panasonic
21	1	R11	RES, 100 Ω, 1%, 1/8 W, Thick Film, 0805	ERJ-6ENF1000V	Panasonic
22	1	R12	RES, 562 Ω, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF5620V	Panasonic
23	1	R13	RES, 6.2 kΩ, 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ622V	Panasonic
24	1	RV1	Varistor, 350 VAC, 3.5 K A, 10.5 mm, Bulk ZNR, ERZ-E, Surge Absorber	ERZ-E08A561	Panasonic
25	1	T1	Bobbin, EFD25, Horizontal, 10 pins		
26	1	U1	LinkSwitch-XT2, DIP-8C	LNK3696P	Power Integrations
27	1	U3	Optocoupler, 35 V, CTR 80-160%, 4-DIP	LTV-817A	Liteon
28	1	VR1	Diode, Zener, 17 V, ±5%, 500 mW, SOD123, SOD-123	MMSZ5247BT1G	ON Semi

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	JP1	Wire Jumper, Insulated, #24 AWG, 0.4 in	C2003A-12-02	Gen Cable
2	1	L	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
3	1	N	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
4	1	VOUT2	Test Point, YEL, THRU-HOLE MOUNT	5014	Keystone
5	1	RTN2	Test Point, BLU, THRU-HOLE MOUNT	5127	Keystone
6	1	VOUT1	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
7	1	RTN1	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone

7 Transformer Specification

7.1 Electrical Diagram

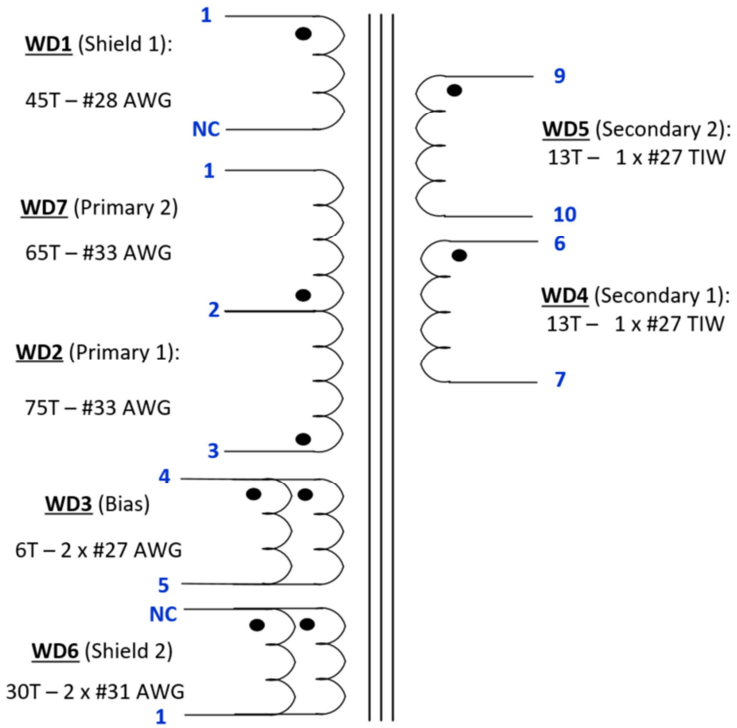


Figure 6 – Transformer Electrical Diagram.

7.2 Electrical Specifications

Parameter	Condition	Spec
Primary Inductance	Pins 1-3, all other windings open, measured at 100 kHz, 1.0 V_{RMS}.	4014 µH ±10%
Primary Leakage Inductance	Pins 1-3, all other windings short, measured at 100 kHz, 1.0 V_{RMS}.	<100 µH

7.3 Material List

Item	Description
[1]	Core: EFD25, Gapped.
[2]	Bobbin: EFD25, Horizontal, 10 Pins. PI #25-00047-00
[3]	Magnet Wire: #33 AWG, Double Coated.
[4]	Magnet Wire: #31 AWG, Double Coated.
[5]	Magnet Wire: #28 AWG, Double Coated.
[6]	Magnet Wire: #27 AWG, Double Coated.
[7]	Magnet Wire: #27 AWG, Triple Insulated Wire.
[8]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 17.5 mm Wide.
[9]	Tape, 3M 1298 Polyester Film, 2.0 Mils Thick, 9 mm Wide.
[10]	Varnish.

7.4 Transformer Build Diagram

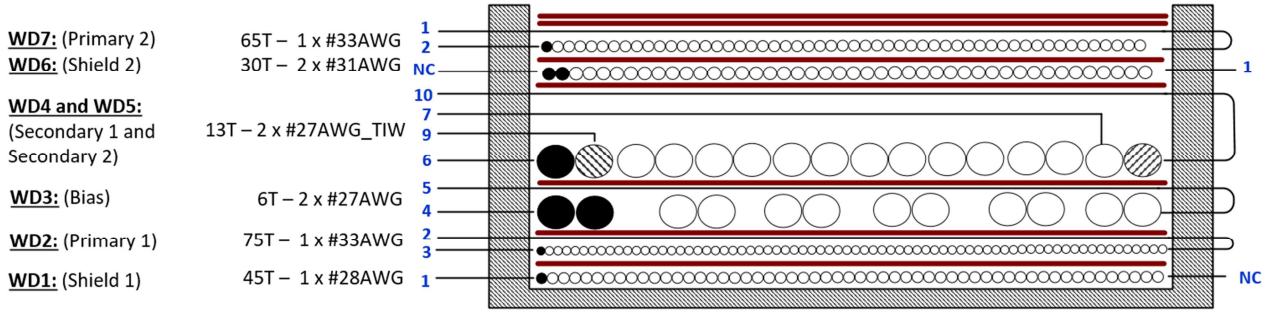
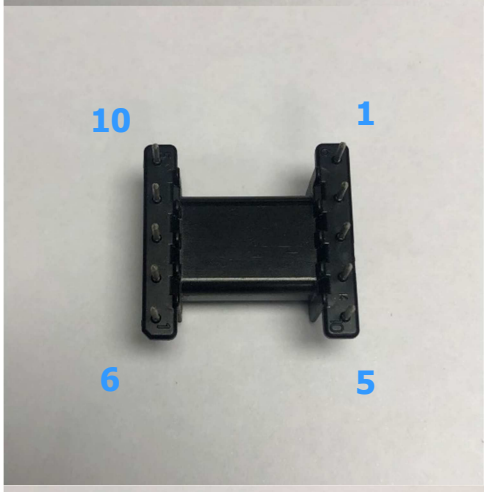
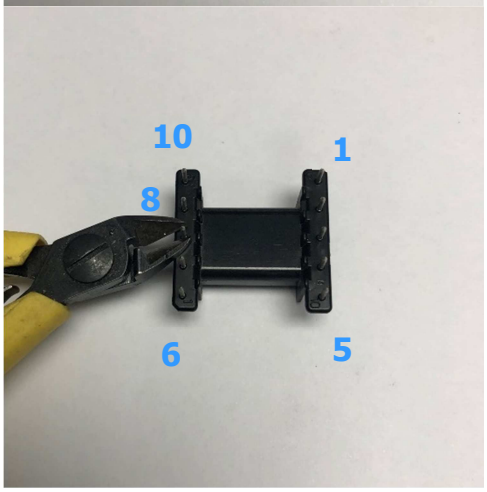


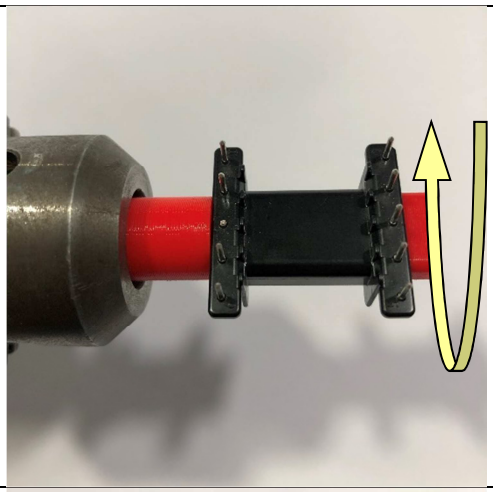
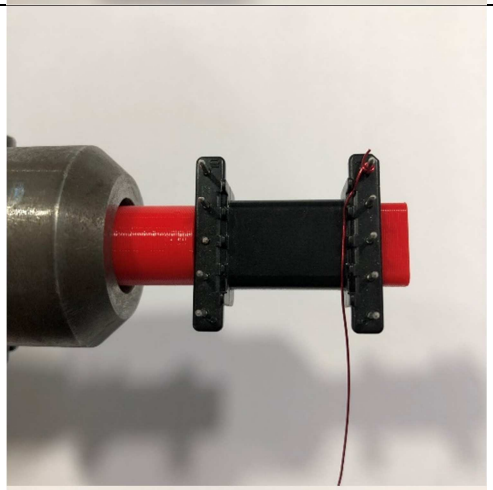
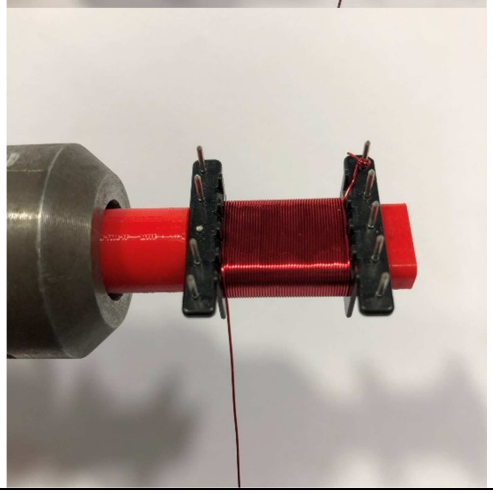
Figure 7 – Transformer Build Diagram.

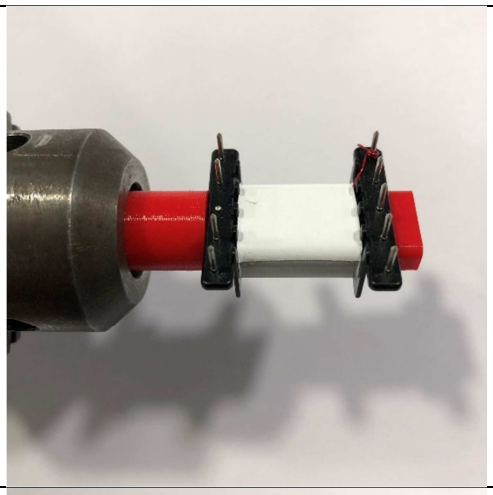
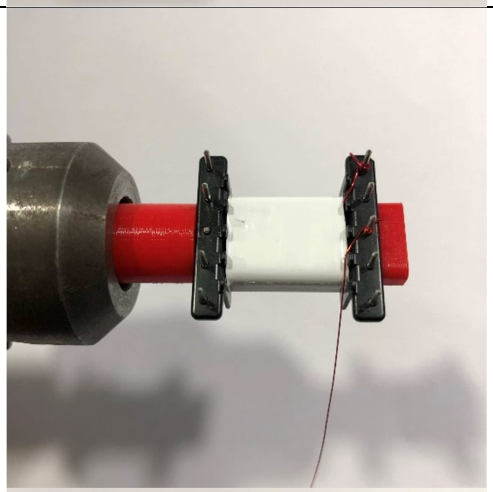
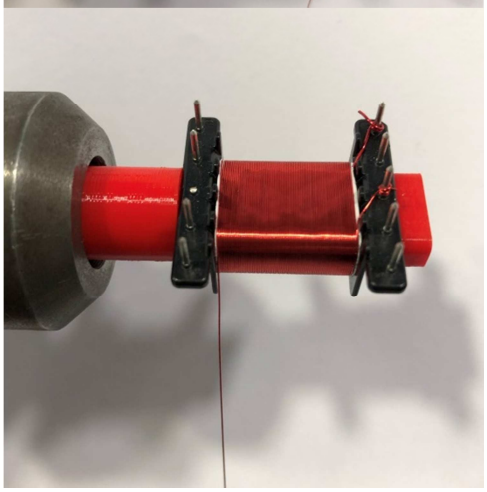
7.5 Transformer Construction

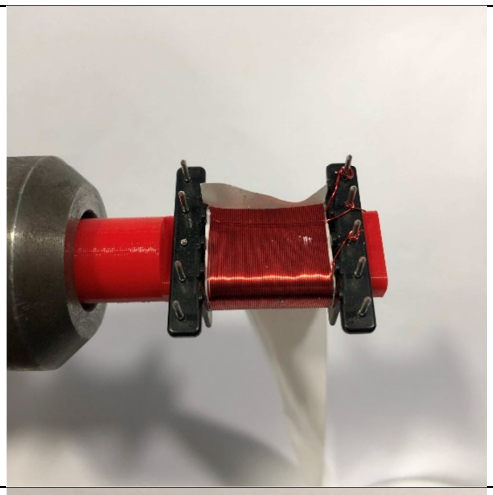
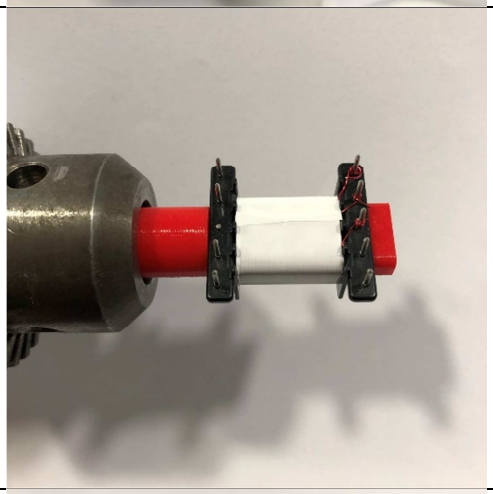
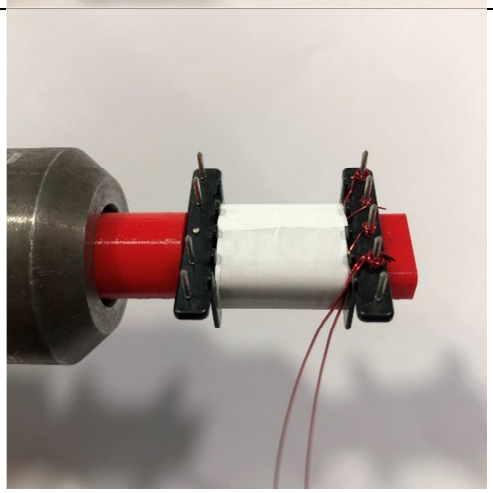
Winding Preparation	Remove pin 8 from the bobbin Item [2]. Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
WD1 Shield 1	Starting at pin 1, wind 45 turns of wire Item [5] in one layer. Terminate at the end. (NC)
Insulation	Apply one layer of tape Item [8] for insulation.
WD2 Primary 1	Starting at pin 3, wind 75 turns of wire Item [3] in one layer. At the last turn, bring the wire back across the windings and terminate at pin 2.
Insulation	Apply one layer of tape Item [8] for insulation.
WD3 Bias	Start at pin 4, wind 6 bifilar turns of wire Item [6] in one layer. Spread the turns evenly across the winding area. At the last turn, bring the wires back across the windings and terminate at pin 5.
Insulation	Apply one layer of tape Item [8] for insulation.
WD4 and WD5 Vout 1 and Vout 2	Tie a knot at the end of one of the two wires Item [7] to indicate if it is for WD4 (starts at pin 6, is terminated at pin 7) or WD5 (starts at pin 9, is terminated at pin 10). Starting at pin 6 and pin 9, wind 13 bifilar turns of wire Item [7] in one layer. At the last turn, bring the wires back across the winding. For WD4, which started at pin 6, terminate at pin 7. For WD5, which started at pin 9, terminate at pin 10.
Insulation	Apply one layer of tape Item [8] for insulation.
WD6 Shield 2	Place the bobbin Item [2] such that pins 1-5 are facing the winder. Winding direction is counter-clockwise as shown. Start at pin 1, wind 30 bifilar turns of wire Item [4] in one layer. Terminate at the end (NC).
Insulation	Apply one layer of tape Item [8] for insulation.
WD7 Primary 2	Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown. Start at pin 2, wind 65 turns of wire Item [3] in one layer. At the last turn, bring the wire back across the windings and terminate at pin 1.
Insulation	Apply two layers of tape Item [8] for insulation.
Assembly	Grind core halves to get 4.01 mH primary inductance. Secure core halves with 1 layer of tape Item [9]. Reduce pin 2 from the bobbin Item [2]. Dip in varnish Item [10]. Fill in vias with solder as shown.

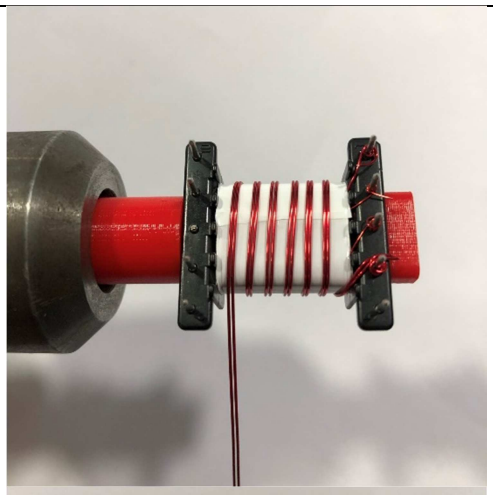
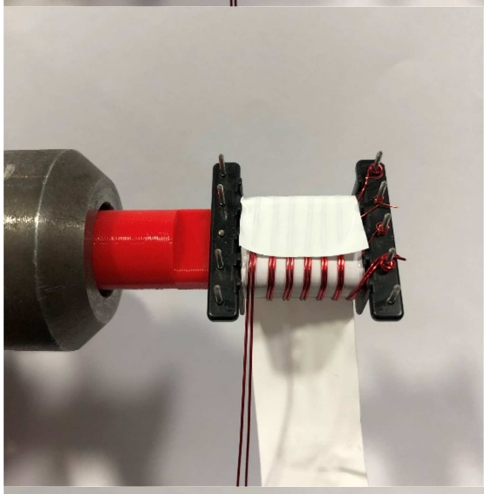
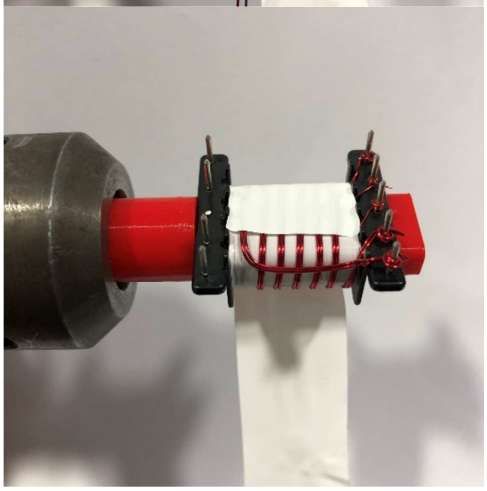
7.6 Transformer Winding Illustrations

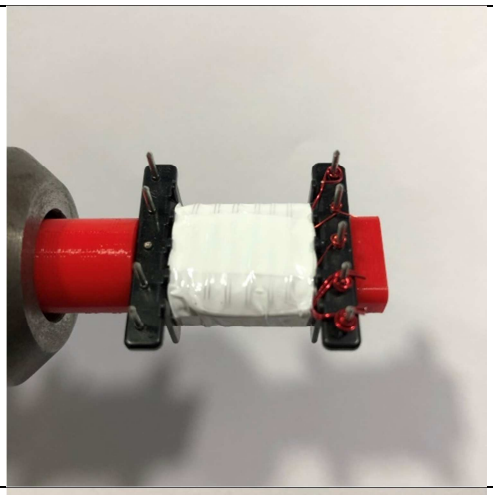
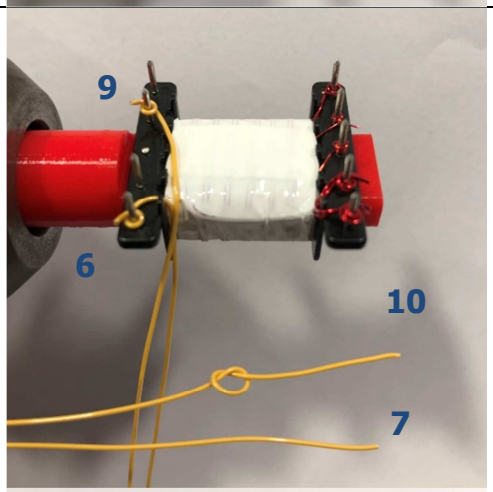
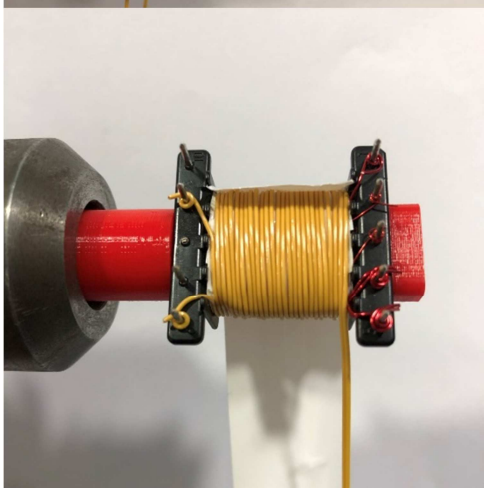
Winding Preparation	  	Remove pin 8 from the bobbin Item [2].

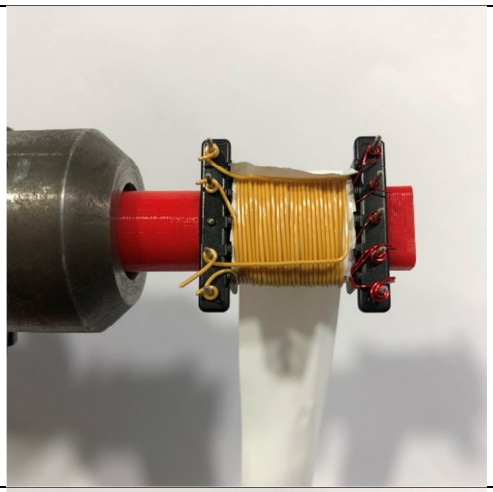
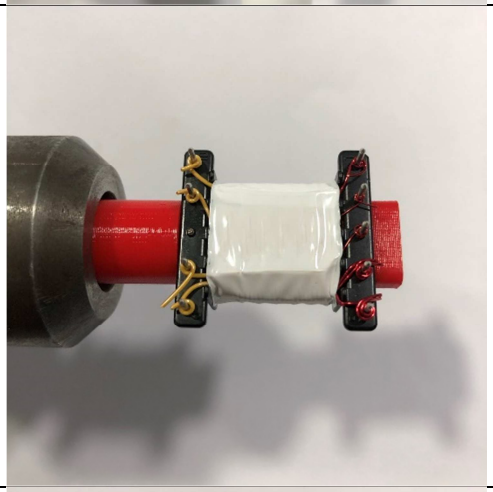
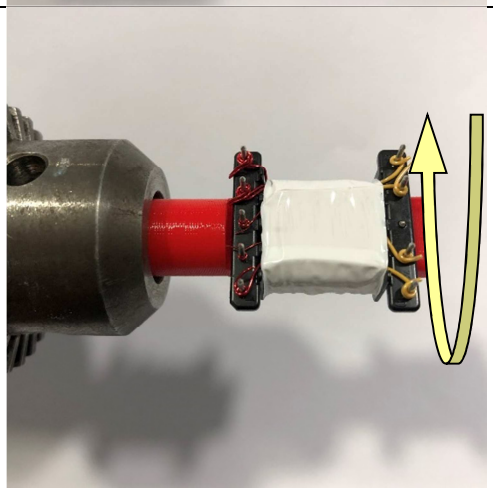
		Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
WD1 **Shield 1**	 	Starting at pin 1, wind 45 turns of wire Item [5] in one layer. Terminate at the end. (NC)

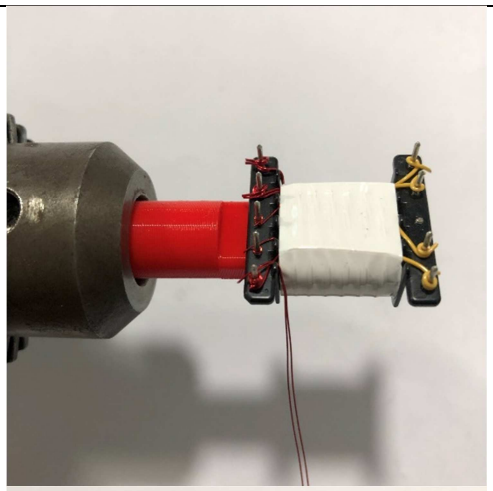
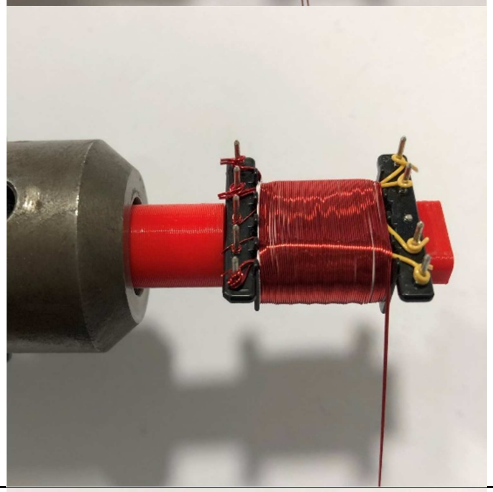
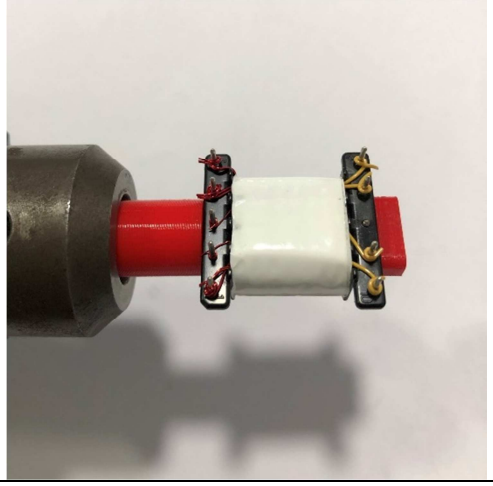
Insulation		Apply one layer of tape Item [8] for insulation.
WD2 **Primary 1**	 	Starting at pin 3, wind 75 turns of wire Item [3] in one layer.

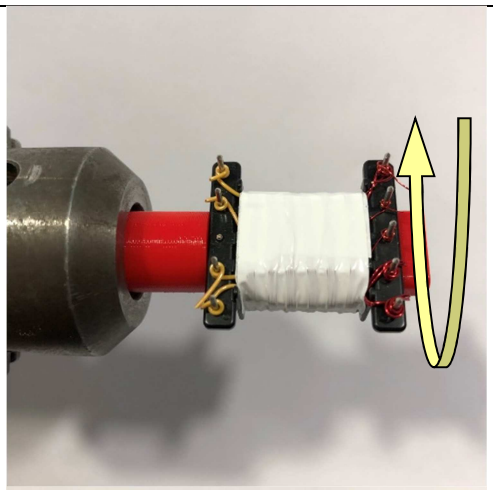
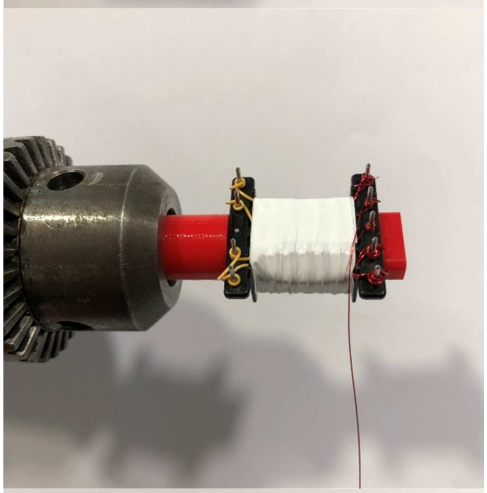
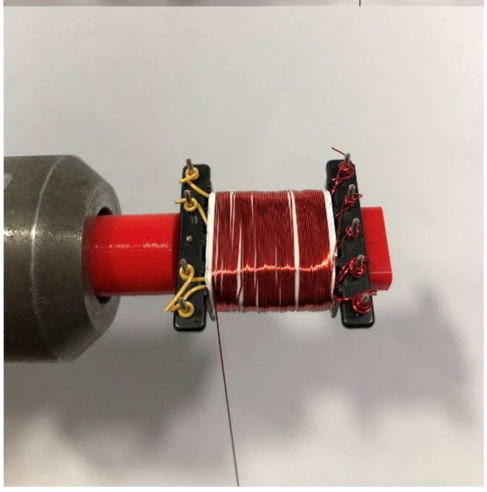
		At the last turn, bring the wire back across the windings and terminate at pin 2.
Insulation		Apply one layer of tape Item [8] for insulation.
WD3 Bias		Start at pin 4, wind 6 bifilar turns of wire Item [6] in one layer.

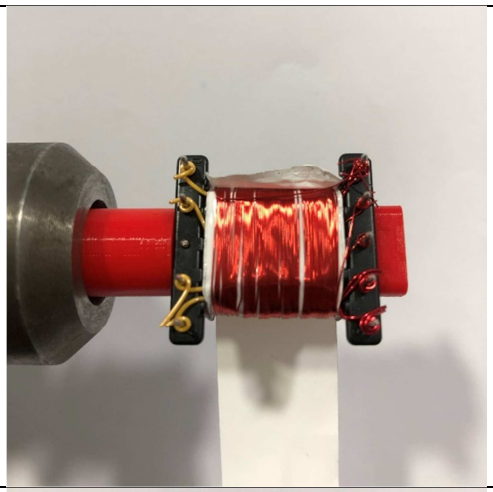
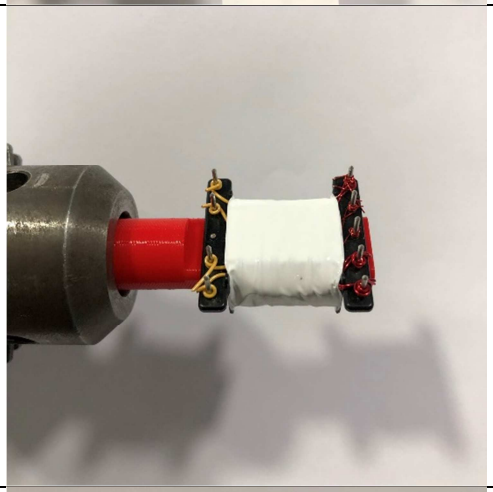
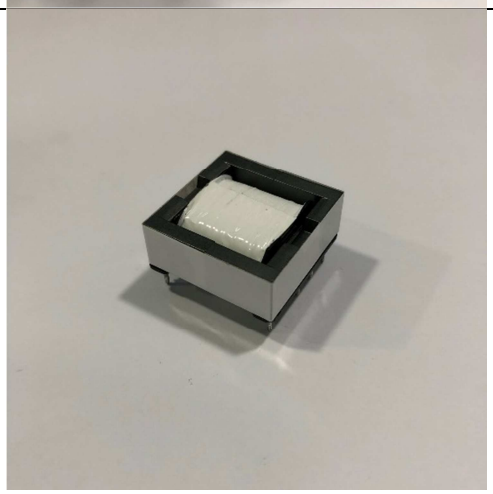
		Spread the turns evenly across the winding area.
		
		At the last turn, bring the wires back across the windings and terminate at pin 5.

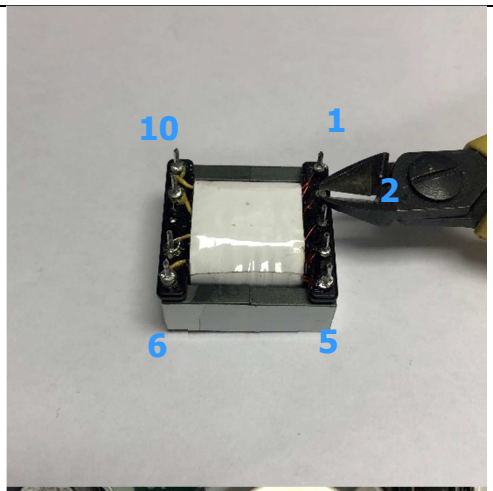
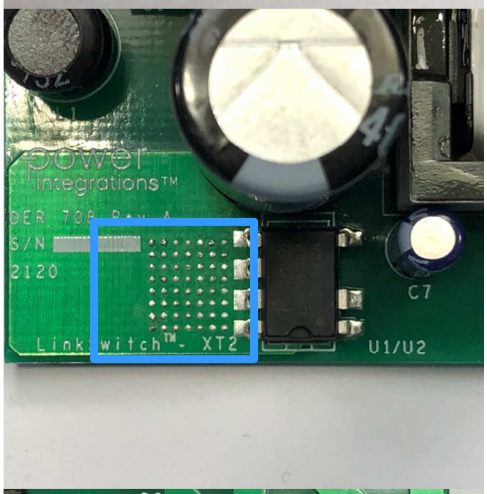
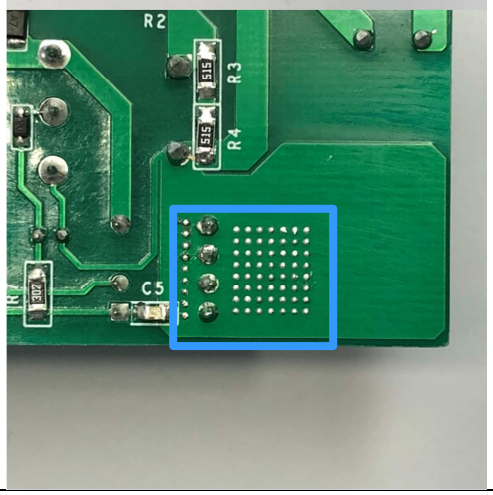
Insulation		Apply one layer of tape Item [8] for insulation.
WD4 and WD5 Vout 1 and Vout 2	 	Tie a knot at the end of one of the two wires Item [7] to indicate if it is for WD4 (starts at pin 6, is terminated at pin 7) or WD5 (starts at pin 9, is terminated at pin 10). Starting at pin 6 and pin 9, wind 13 bifilar turns of wire Item [7] in one layer.

		At the last turn, bring the wires back across the winding. For WD4, which started at pin 6, terminate at pin 7. For WD5, which started at pin 9, terminate at pin 10.
Insulation		Apply one layer of tape Item [8] for insulation.
WD6 **Shield 2**		Place the bobbin Item [2] such that pins 1-5 are facing the winder. Winding direction is counter-clockwise as shown.

		Start at pin 1, wind 30 bifilar turns of wire Item [4] in one layer.
		Terminate at the end (NC).
Insulation		Apply one layer of tape Item [8] for insulation.

WD7 **Primary 2**		Place the bobbin Item [2] such that pins 6-10 are facing the winder. Winding direction is counter-clockwise as shown.
		Start at pin 2, wind 65 turns of wire Item [3] in one layer.
		

		At the last turn, bring the wire back across the windings and terminate at pin 1.
Insulation		Apply two layers of tape Item [8] for insulation.
Assembly		Grind core halves to get 4.01 mH primary inductance. Secure core halves with 1 layer of tape Item [9].

	  	Reduce pin 2 from the bobbin Item [2]. Dip in varnish Item [10]. Fill in vias with solder as shown.

8 Transformer Design Spreadsheet

Note: The output current entered in the spreadsheet was increased such that POUT matches the combined power of the dual outputs.

ACDC_LinkSwitchXT2 900V_092018; Rev.1.1; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNIT	ACDC_LinkSwitchXT2 900V Flyback Design Spreadsheet
ENTER APPLICATION VARIABLES					
LINE VOLTAGE RANGE			UNIVERSAL		AC line voltage range
VACMIN	85.00		85.00	Volts	Minimum AC line voltage
VACTYP	230.00		230.00	Volts	Typical AC line voltage
VACMAX	350.00		350.00	Volts	Maximum AC line voltage
fL			50	Hertz	AC mains frequency
TIME_BRIDGE_CONDUCTION			2.39	mseconds	Input bridge rectifier diode conduction time
LINE RECTIFICATION			F		Select 'F'ull wave rectification or 'H'alf wave rectification
VOUT	18.00		18.00	Volts	Output voltage
IOUT	0.550		0.550	Amperes	Average output current specification
EFFICIENCY			0.80		Efficiency Estimate at output terminals. Under 0.8 if no better data available
LOSS ALLOCATION FACTOR			0.50		The ratio of power losses during the MOSFET off-state to the total system losses
POUT		Warning	9.90	Watts	Device maximum power capability has been exceeded. Verify thermal performance
CIN	41.00		41.00	uFarads	Input capacitor
VMIN			97.57	Volts	Valley of the rectified VACMIN
VMAX			494.97	Volts	Peak of the VACMAX
FEEDBACK	OPTO		OPTO		Select the type of feedback required. (OPTO = feedback via Optocoupler Network)
BIAS WINDING	YES		YES		Select whether a bias winding is required
LINKSWITCH-XT2 VARIABLES					
CURRENT LIMIT MODE			STD		Pick between 'RED' (Reduced) or 'STD' (Standard) current limit mode of operation
PACKAGE			DIP-8C		Device package
ENCLOSURE			OPEN FRAME		Device enclosure
GENERIC DEVICE	LNK3696		LNK3696		Device series
DEVICE CODE			LNK3696P		Device code
PMAX			8.00	Watts	Device maximum power capability
VOR	200		200	Volts	Voltage reflected to the primary winding when the MOSFET is off
VDSON			10.0	Volts	MOSFET on-time drain to source peak voltage
VDSOFF			795.0	Volts	Estimated MOSFET drain-to-source voltage during Off-time
ILIMITMIN			0.446	Amperes	Minimum current limit
ILIMITTYP			0.482	Amperes	Typical current limit
ILIMITMAX			0.518	Amperes	Maximum current limit
FSMIN			62000	Hertz	Minimum switching frequency
FSTYP			66000	Hertz	Typical switching frequency
FSMAX			70000	Hertz	Maximum switching frequency
RDSON			9.70	Ohms	MOSFET drain to source resistance at 25degC
PRIMARY WAVEFORM PARAMETERS					
MODE OF OPERATION			DCM		Mode of operation
KRP/KDP			1.320		Measure of continuous/discontinuous mode of operation

KP_TRANSIENT			1.069		KP under conditions of a transient
DMAX			0.634		Maximum duty cycle at VMIN
TIME_ON			10.221	useconds	MOSFET conduction time at the minimum line voltage
TIME_ON_MIN			1.748	useconds	MOSFET conduction time at the maximum line voltage
IAVG_PRIMARY			0.141	Amperes	Average input current
IRMS_PRIMARY			0.205	Amperes	Root mean squared value of the primary current
LPRIMARY_MIN			1806	uH	Minimum primary inductance
LPRIMARY_TYP			2007	uH	Typical primary inductance
LPRIMARY_MAX			2208	uH	Maximum primary inductance
LPRIMARY_TOL			10		Tolerance of the Primary inductance
SECONDARY WAVEFORM PARAMETERS					
IPEAK_SECONDARY			5.578	Amperes	Peak secondary current
IRMS_SECONDARY			1.697	Amperes	Root mean squared value of the secondary current
PIV_SECONDARY			63.96	Volts	Peak inverse voltage on the secondary diode, not including the leakage spike
VF_SECONDARY			0.70	Volts	Secondary diode forward voltage drop
TRANSFORMER CONSTRUCTION PARAMETERS					
Core selection					
CORE	Custom		Custom		Select the transformer core
BOBBIN	EFD25		EFD25		Bobbin name
AE	58.00		58.00	mm^2	Cross sectional area of the core
LE	57.00		57.00	mm	Effective magnetic path length of the core
AL	2000.0		2000.0	nH/(turns^2)	Ungapped effective inductance of the core
VE	3300.0		3300.0	mm^3	Volume of the core
AW	40.70		40.70	mm^2	Window area of the bobbin
BW	16.10		16.10	mm	Width of the bobbin
MLT	50.00		50.00	mm	Mean length per turn of the bobbin
MARGIN			0.00	mm	Safety margin
Primary winding					
NPRIMARY			140		PrImary number of turns
BMAX_TARGET			1500	Gauss	Target value of the magnetic flux density
BMAX_ACTUAL			1280	Gauss	Actual value of the magnetic flux density
BAC			640	Gauss	AC flux density
ALG			102	nH/T^2	Gapped core effective inductance
LG			0.675	mm	Core gap length
LAYERS_PRIMARY			2		Number of primary layers
AWG_PRIMARY			33		Primary winding wire AWG
OD_PRIMARY_INSULATED			0.219	mm	Primary winding wire outer diameter with insulation
OD_PRIMARY_BARE			0.180	mm	Primary winding wire outer diameter without insulation
CMA_PRIMARY			245	mil^2/Amperes	Primary winding wire CMA
Secondary winding					
NSECONDARY			13		Secondary turns
AWG_SECONDARY			24		Secondary winding wire AWG
OD_SECONDARY_INSULATED			0.815	mm	Secondary winding wire outer diameter with insulation
OD_SECONDARY_BARE			0.511	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			238	mil^2/Amperes	Secondary winding CMA
Bias winding					
NBIAS	6		6		Bias turns
VF_BIAS			0.70	Volts	Bias diode forward voltage drop
VBIAS		Warning	8.63	Volts	Increase the bias winding turns to

					ensure VBIAS > 12V
PIVB			29.84	Volts	Peak inverse voltage on the bias diode
CBP			0.1	uF	BP pin capacitor
FEEDBACK PARAMETERS					
DIODE_BIAS			1N4003-4007		Recommended diode is 1N4003. Place diode on return leg of bias winding for optimal EMI
RUPPER			500 - 1000	ohms	CV bias resistor for CV/CC circuit. See LinkSwitch-XT2 Design Guide
RLOWER			200 - 820	ohms	Resistor to set CC linearity for CV/CC circuit. See LinkSwitch-XT2 900V Design Guide
MULTIPLE OUTPUT PARAMETERS					
Output 1					
VOUT1			18.00	Volts	Output Voltage 1
IOUT1	0.300		0.300	Amperes	Output Current 1
POUT1			5.40	Watts	Output Power 1
VD1			0.70	Volts	Secondary diode forward voltage drop for output 1
NS1			13		Number of turns for output 1
ISRMS1			0.925	Amperes	Root mean squared value of the secondary current for output 1
IRIPPLE1			0.875	Amperes	Current ripple on the secondary waveform for output 1
PIV1			63.96	Volts	Peak inverse voltage on the secondary diode for output 1
DIODE1_RECOMMENDED			SB1100		Recommended diode for output 1
PRELOAD			N/A	kohms	Preload resistor to ensure a load of at least 3mA on the first output for BIAS, 2mA for MAIN
CMS1			185.1	Cmils	Bare conductor effective area in circular mils for output 1
AWGS1			27	AWG	Wire size for output 1
Output 2					
VOUT2	18.00		18.00	Volts	Output Voltage 2
IOUT2	0.250		0.250	Amperes	Output Current 2
POUT2			4.50	Watts	Output Power 2
VD2			0.70	Volts	Secondary diode forward voltage drop for output 2
NS2			13		Number of turns for output 2
ISRMS2			0.771	Amperes	Root mean squared value of the secondary current for output 2
IRIPPLE2			0.729	Amperes	Current ripple on the secondary waveform for output 2
PIV2			63.96	Volts	Peak inverse voltage on the secondary diode for output 2
DIODE2_RECOMMENDED			SB1100		Recommended diode for output 2
CMS2			154.2	Cmils	Bare conductor effective area in circular mils for output 2
AWGS2			28	AWG	Wire size for output 2
Output 3					
VOUT3			0.00	Volts	Output Voltage 3
IOUT3			0.000	Amperes	Output Current 3
POUT3			0.00	Watts	Output Power 3
VD3			0.70	Volts	Secondary diode forward voltage drop for output 3
NS3			1		Number of turns for output 3
ISRMS3			0.000	Amperes	Root mean squared value of the secondary current for output 3
IRIPPLE3			0.000	Amperes	Current ripple on the secondary waveform for output 3
PIV3			3.54	Volts	Peak inverse voltage on the secondary

					diode for output 3
DIODE3_RECOMMENDED			NA		Recommended diode for output 3
CMS3			0.0	Cmils	Bare conductor effective area in circular mils for output 3
AWGS3			0	AWG	Wire size output for 3
PO_TOTAL			9.90	Watts	Total power of all outputs
NEGATIVE OUTPUT			N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2

Note:

For the intended application, the typical primary inductance was doubled.

Calculations:
LPRIMARY_TYP (original) = 2007 uH
LPRIMARY_TYP (new) = 4014 uH

BMAX_ACTUAL (original) = 1280 Gauss
BMAX_ACTUAL (new) = (LPRIMARY_TYP) (ILIM) / (NPRIMARY) (AE)
= (4014 uH) (518 mA) / (140 T) (58 mm^2) = 2561 Gauss (< 3000 G)

POUT warning was due to device have exceeded the maximum power capability. Thermal performance was verified in this report. Device thermal data passed 50^oC ambient temperature operation.

The VBIAS field has a "Warning" because the actual bias voltage is only 8V which is lower than the recommended 12V. This was chosen for improved efficiency and no-load performance.

9 Performance Data

9.1 No-Load Input Power

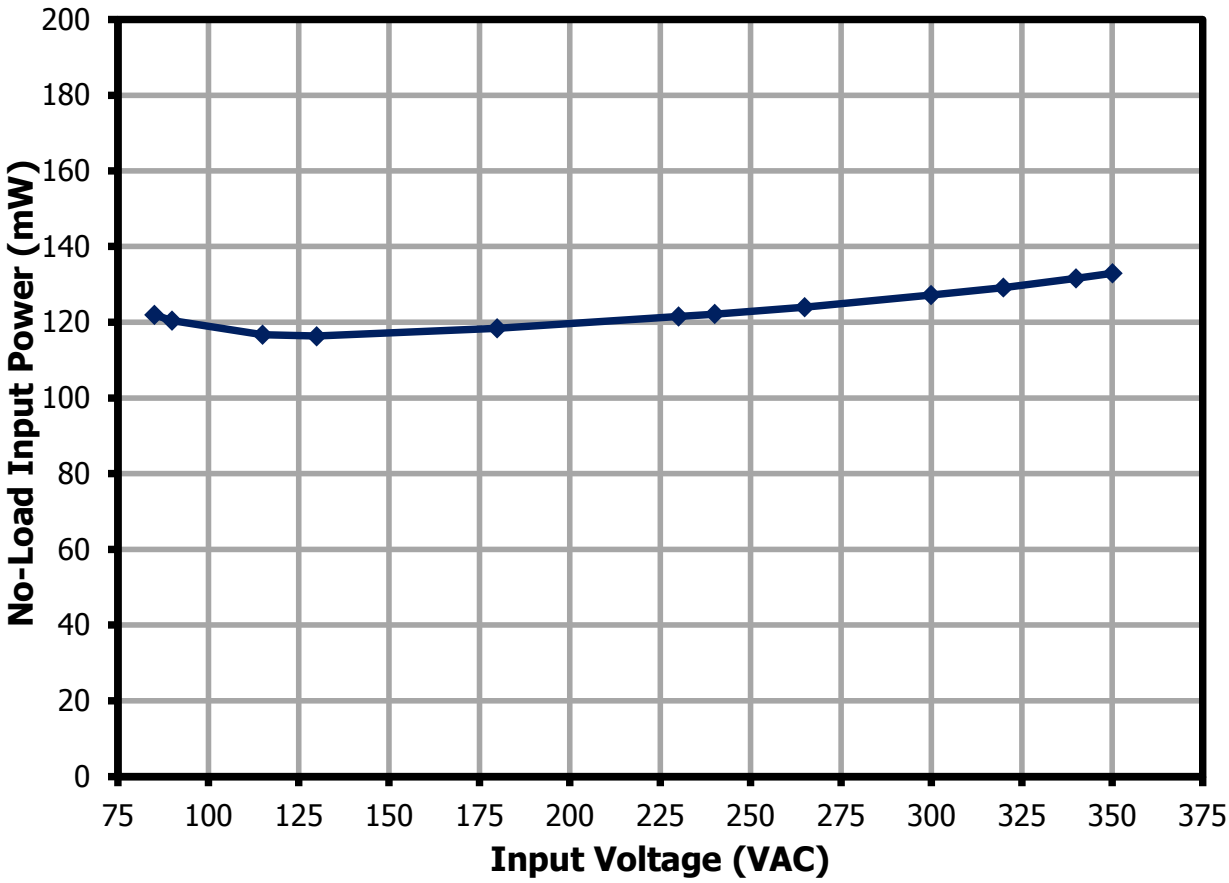


Figure 8 – No-Load Power vs. Input Line Voltage.

9.2 **Efficiency**

9.2.1 *Efficiency vs Line*

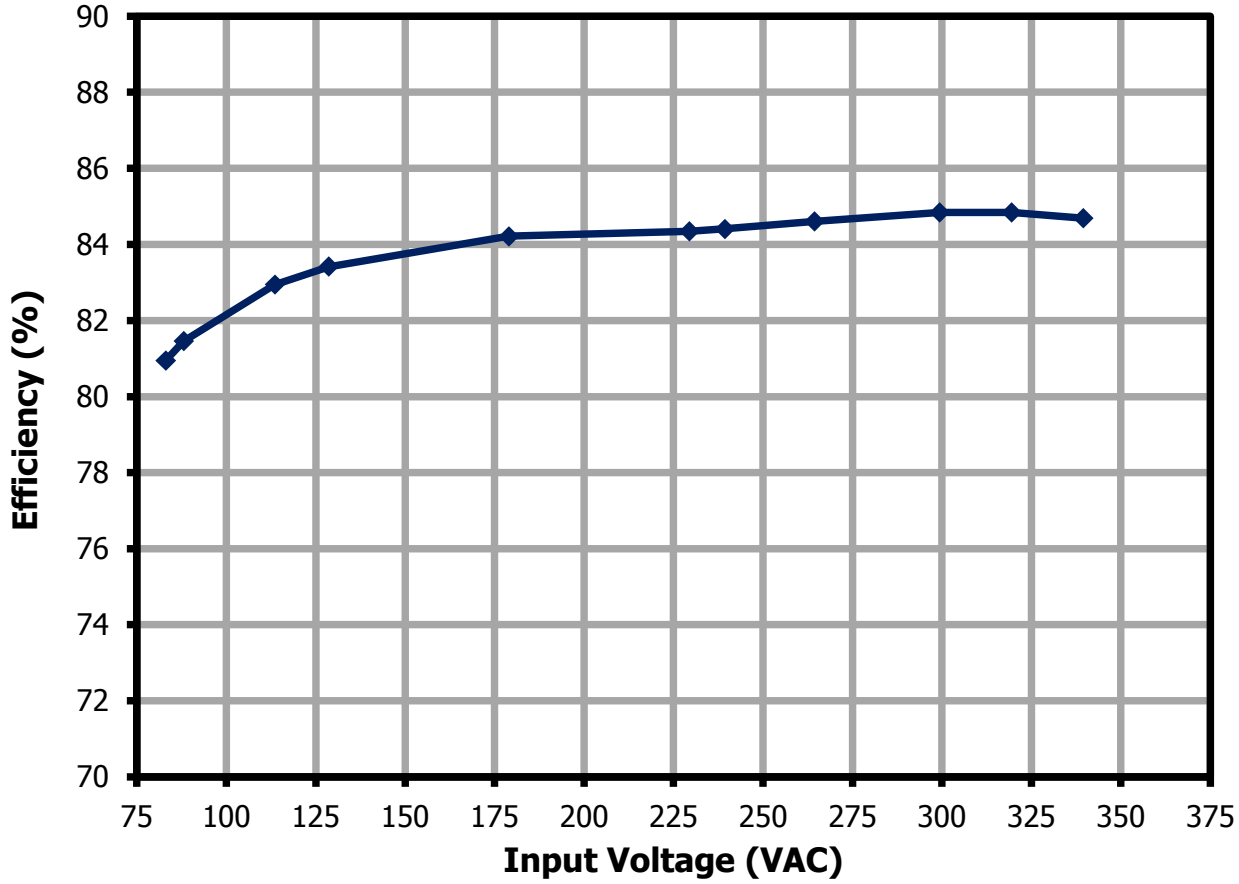


Figure 9 – Full Load Efficiency vs. Input Line Voltage.

9.2.2 *Efficiency vs Load*

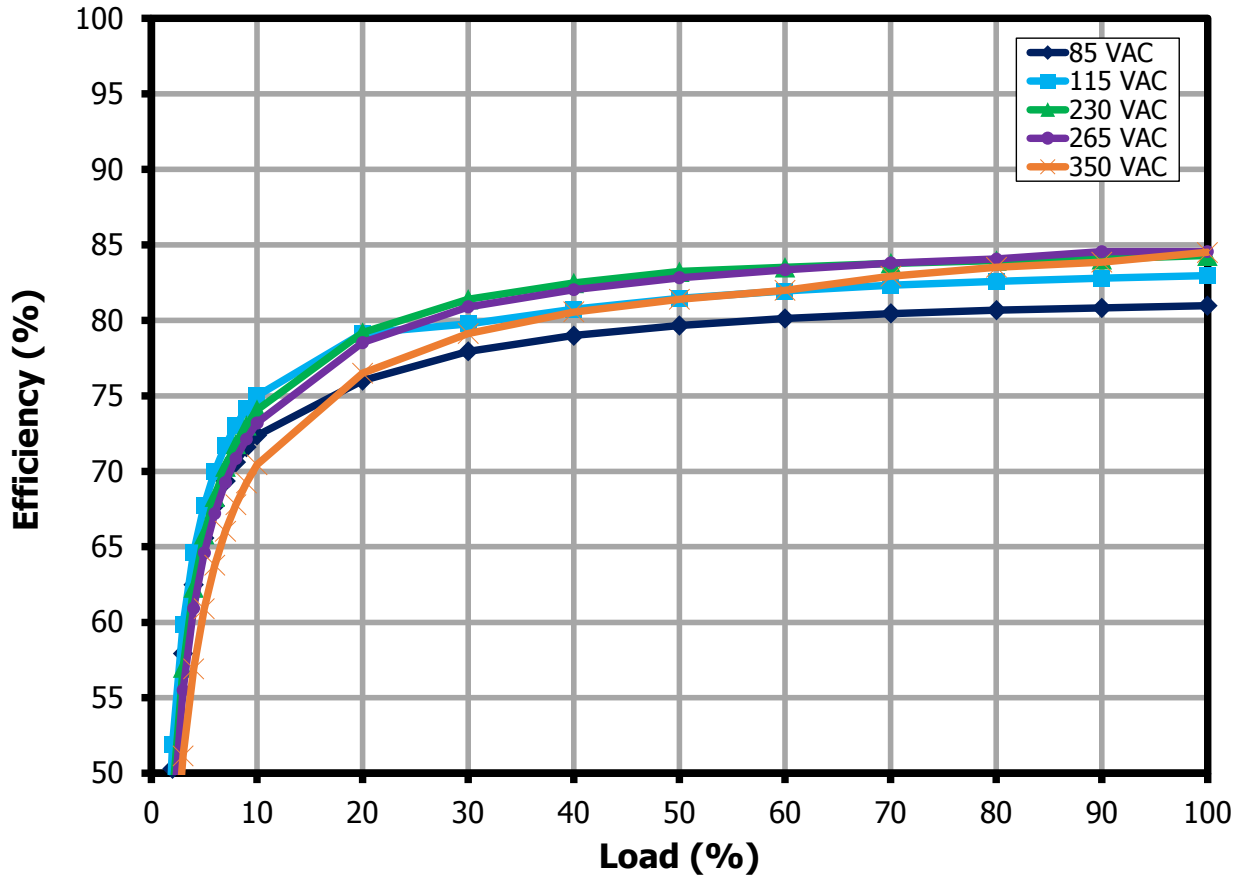


Figure 10 – Efficiency vs. Percent Load, at Different Input Line Voltages.

9.2.3 *Average Efficiency*

9.2.3.1 85 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
83.09	208.27	12.29	18.08	299.61	5.42	18.13	249.91	4.53	80.97
83.56	160.37	9.25	18.08	224.42	4.06	18.13	187.41	3.40	80.59
84.04	111.78	6.23	18.07	149.28	2.70	18.12	124.89	2.26	79.66
84.52	61.28	3.20	18.04	74.00	1.34	18.09	62.40	1.13	77.13
						Average Efficiency			**79.59**

9.2.3.2 115 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
113.63	158.65	12.00	18.09	299.60	5.42	18.15	249.91	4.54	82.97
113.93	122.80	9.04	18.08	224.42	4.06	18.14	187.41	3.40	82.47
114.27	86.09	6.09	18.07	149.28	2.70	18.13	124.89	2.26	81.46
114.63	47.35	3.11	18.06	74.00	1.34	18.11	62.40	1.13	79.25
						Average Efficiency			**81.54**

9.2.3.3 230 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
229.38	90.51	11.81	18.09	299.60	5.42	18.14	249.91	4.53	84.30
229.55	70.58	8.90	18.09	224.42	4.06	18.15	187.41	3.40	83.85
229.73	49.75	5.96	18.07	149.28	2.70	18.13	124.89	2.26	83.23
229.90	28.27	3.06	18.05	74.00	1.34	18.10	62.40	1.13	80.55
						Average Efficiency			**82.98**

9.2.3.4 265 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
264.36	82.61	11.77	18.09	299.58	5.42	18.15	249.91	4.54	84.56
264.51	64.37	8.87	18.08	224.39	4.06	18.14	187.41	3.40	84.11
264.66	45.73	5.99	18.06	149.28	2.70	18.12	124.89	2.26	82.83
264.81	26.10	3.08	18.05	74.00	1.34	18.10	62.40	1.13	79.99
						Average Efficiency			**82.87**

9.2.3.5 350 VAC Input

Input Measurement			Output 1 Measurement			Output 2 Measurement			Efficiency (%)
V_{IN} (RMS)	I_{IN} (mA)	P_{IN} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	V_{OUT} (V)	I_{OUT} (mA)	P_{OUT} (W)	
349.65	67.04	11.78	18.09	299.57	5.42	18.15	249.91	4.54	84.50
349.76	52.94	8.96	18.08	224.38	4.06	18.14	187.41	3.40	83.24
349.87	38.25	6.09	18.07	149.28	2.70	18.12	124.89	2.26	81.40
349.99	22.73	3.15	18.05	73.99	1.34	18.10	62.40	1.13	78.15
						Average Efficiency			**82.82**

9.3 Output Voltage Regulation

9.3.1 *18 V_{OUT1} Load Regulation with Balanced Load*

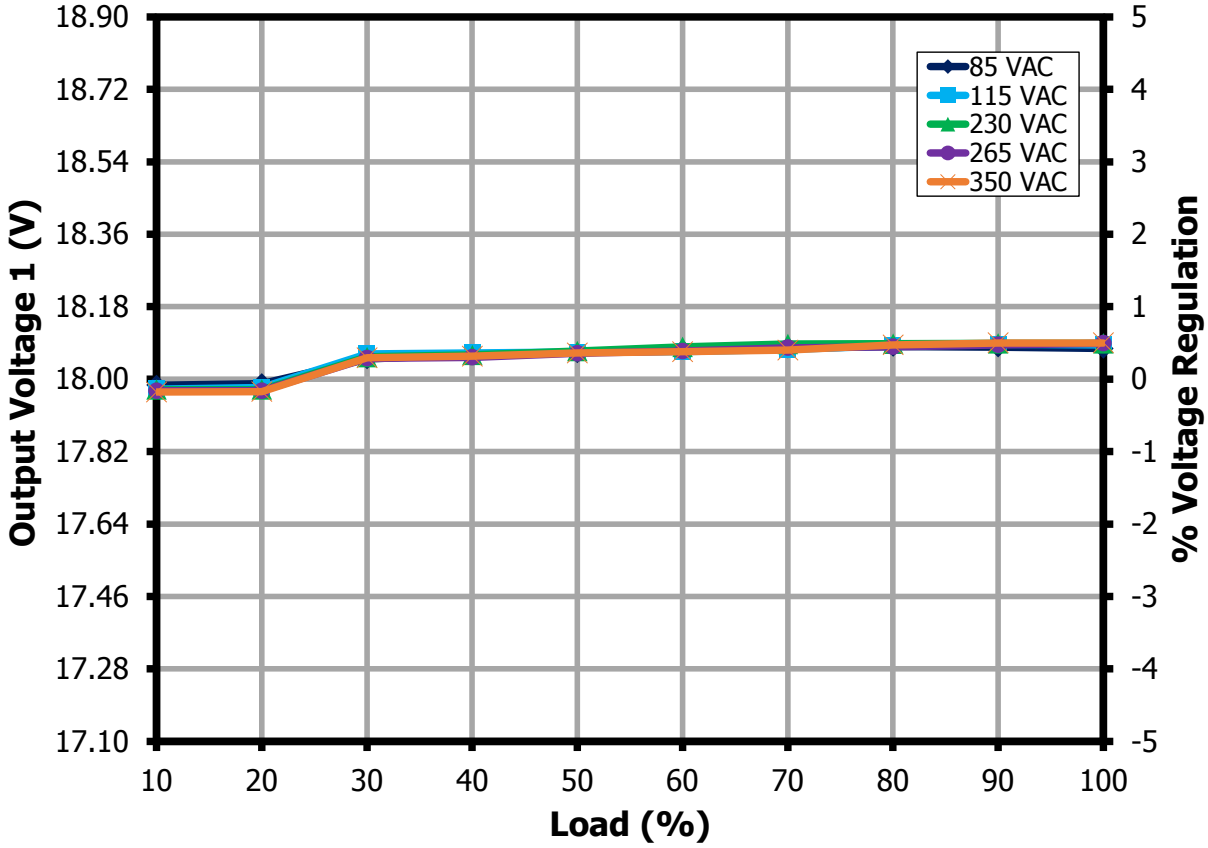


Figure 11 – 18 V_{OUT1} Load Regulation.
Condition: Simultaneous Load Decrement.

9.3.2 *18 V_{OUT2} Load Regulation with Balanced Load*

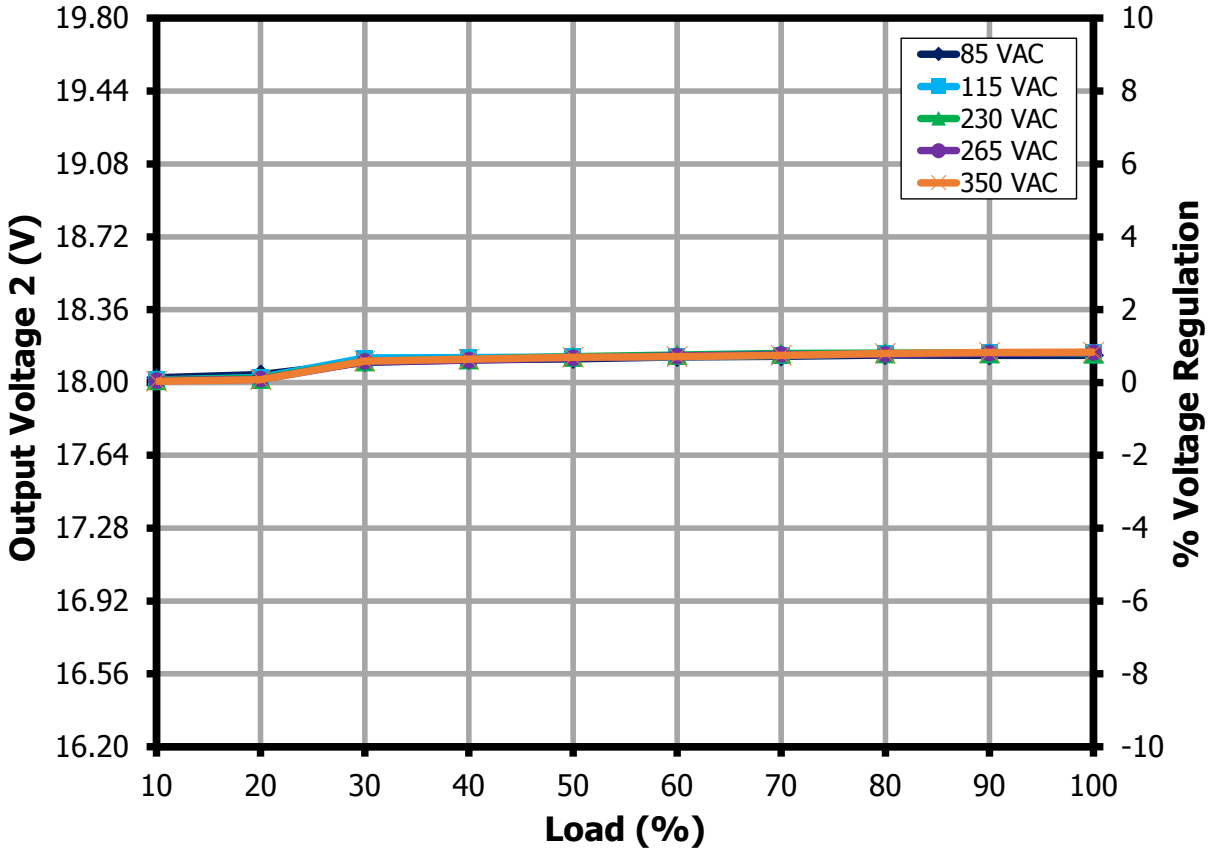


Figure 12 – 18 V_{OUT2} Load Regulation.
Condition: Simultaneous Load Decrement.

9.3.3 *18 V_{OUT1} Load Regulation with Unbalanced Load*

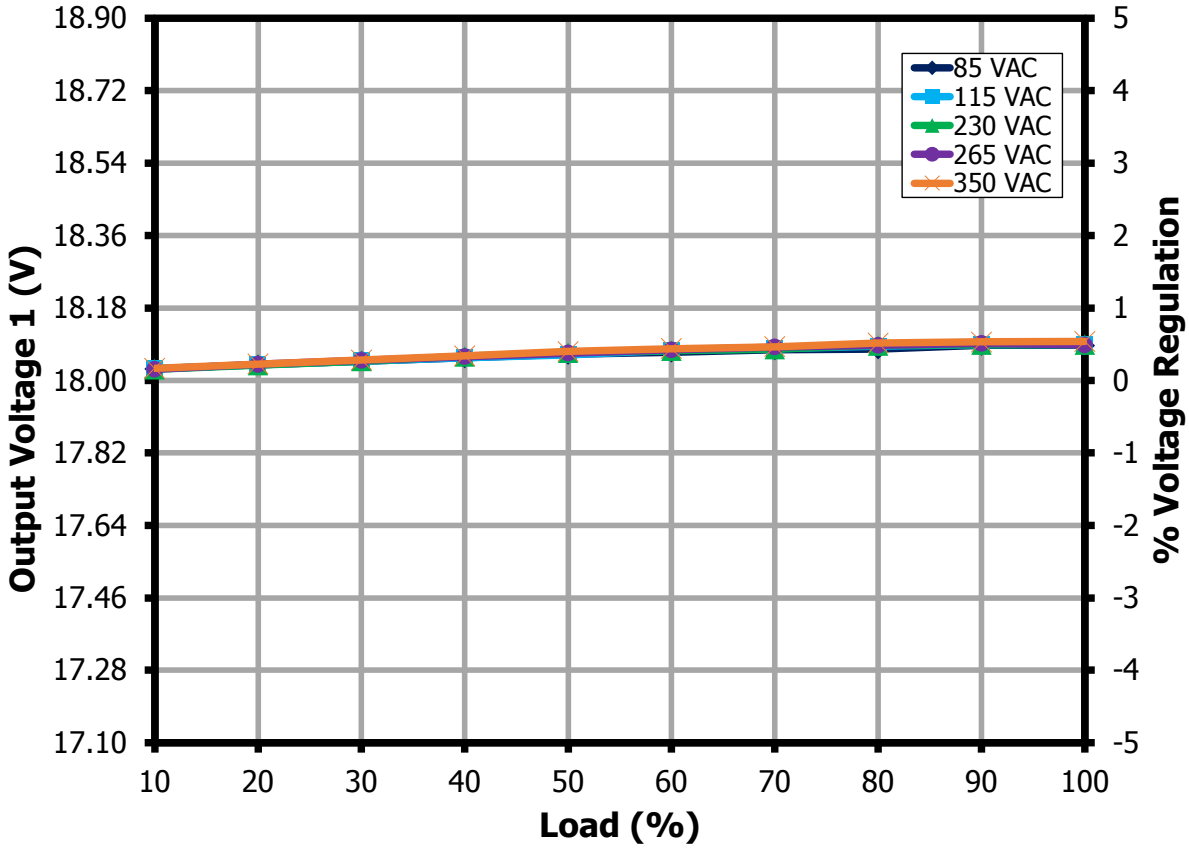


Figure 13 – 18 V_{OUT1} Load Regulation.
Condition: 18 V_{OUT2} at 250 mA, 18 V_{OUT1} Load Sweep.

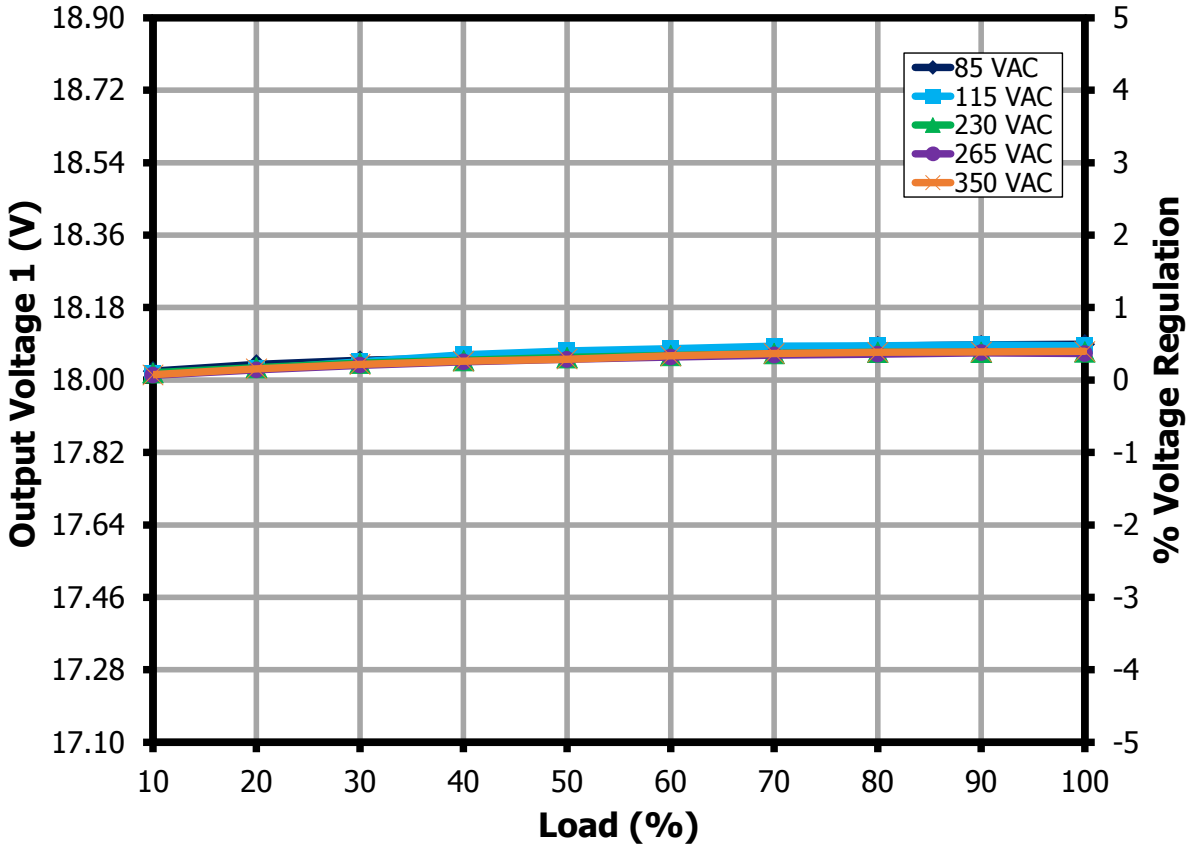


Figure 14 – 18 V_{OUT1} Load Regulation.
Condition: 18 V_{OUT2} at 25 mA, 18 V_{OUT1} Load Sweep.

9.3.4 *18 V_{OUT2} Load Regulation with Unbalanced Load*

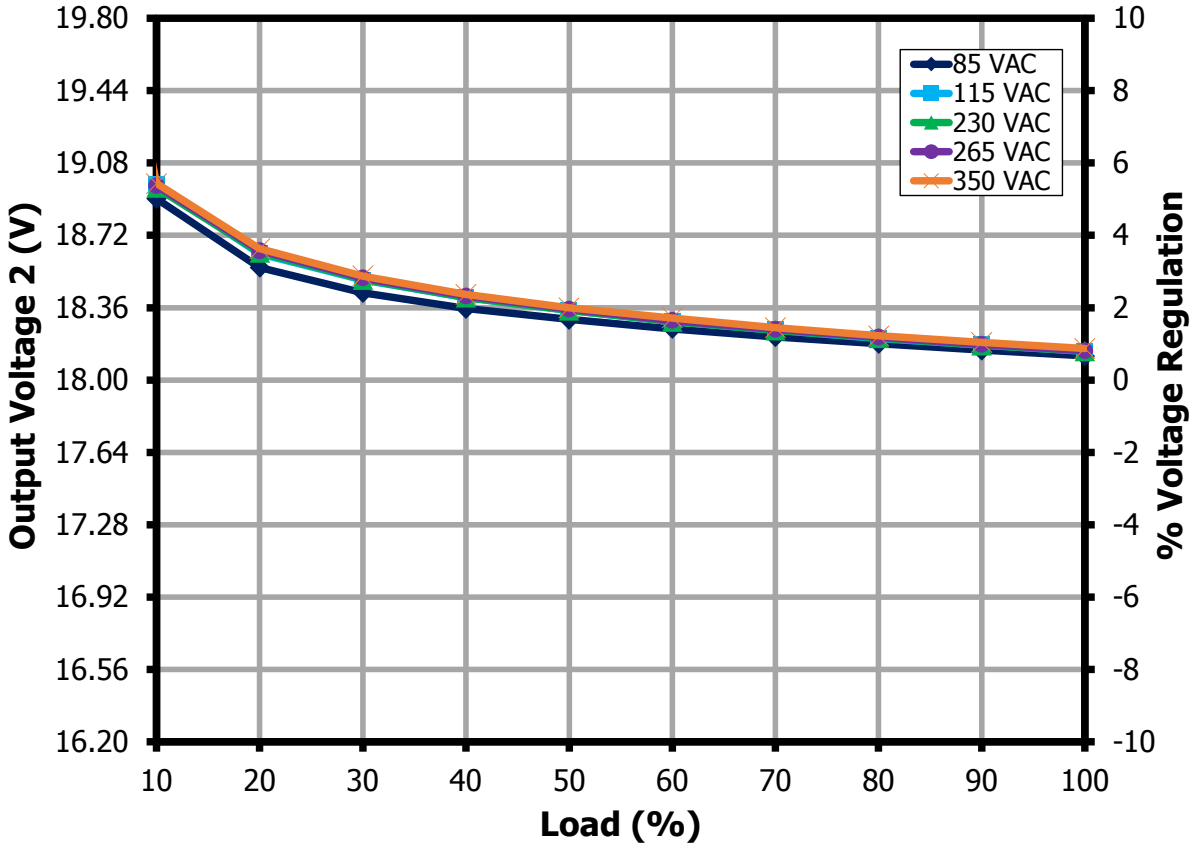


Figure 15 – 18 V_{OUT2} Load Regulation.
Condition: 18 V_{OUT1} at 300 mA, 18 V_{OUT2} Load Sweep.

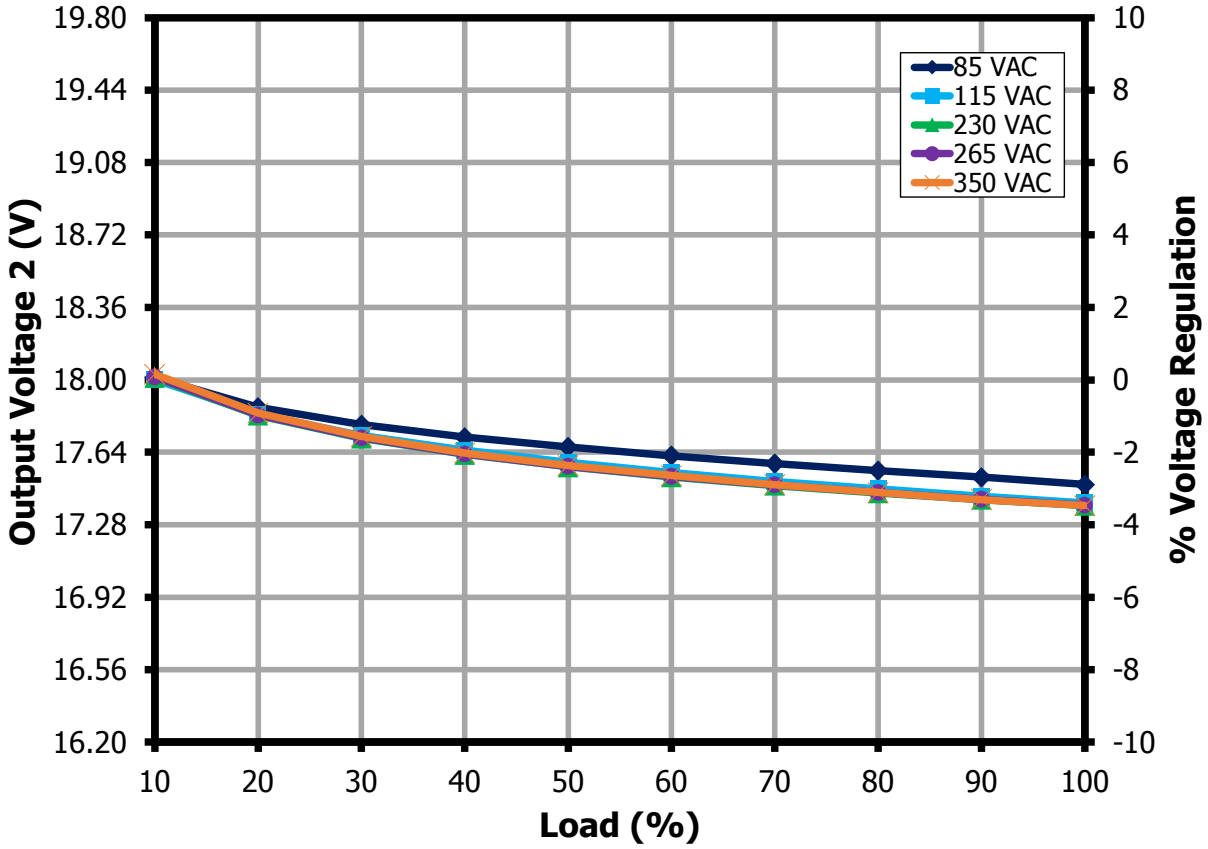


Figure 16 – 18 V_{OUT2} Load Regulation.
Condition: 18 V_{OUT1} at 30 mA, 18 V_{OUT2} Load Sweep.

9.3.5 *Line Regulation*

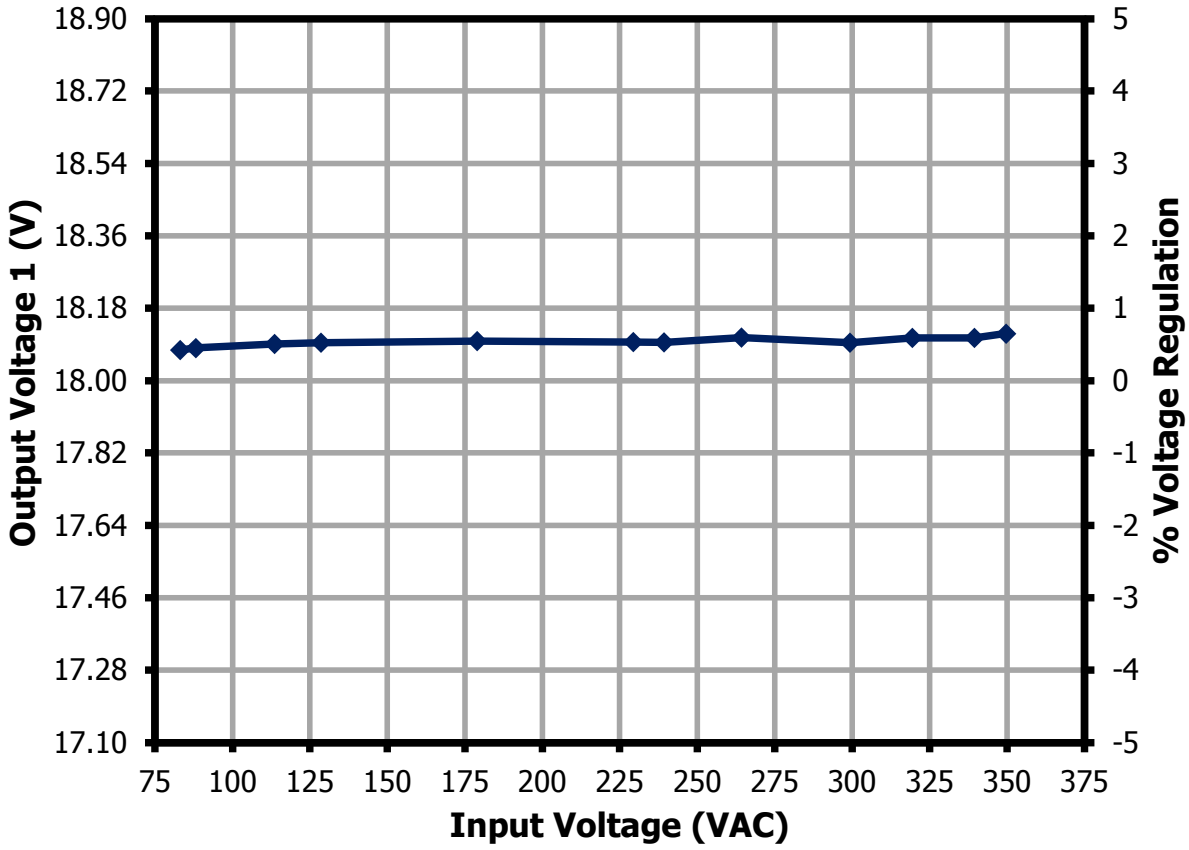


Figure 17 – 18 V_{OUT1} Output Regulation vs. Input Line Voltage.

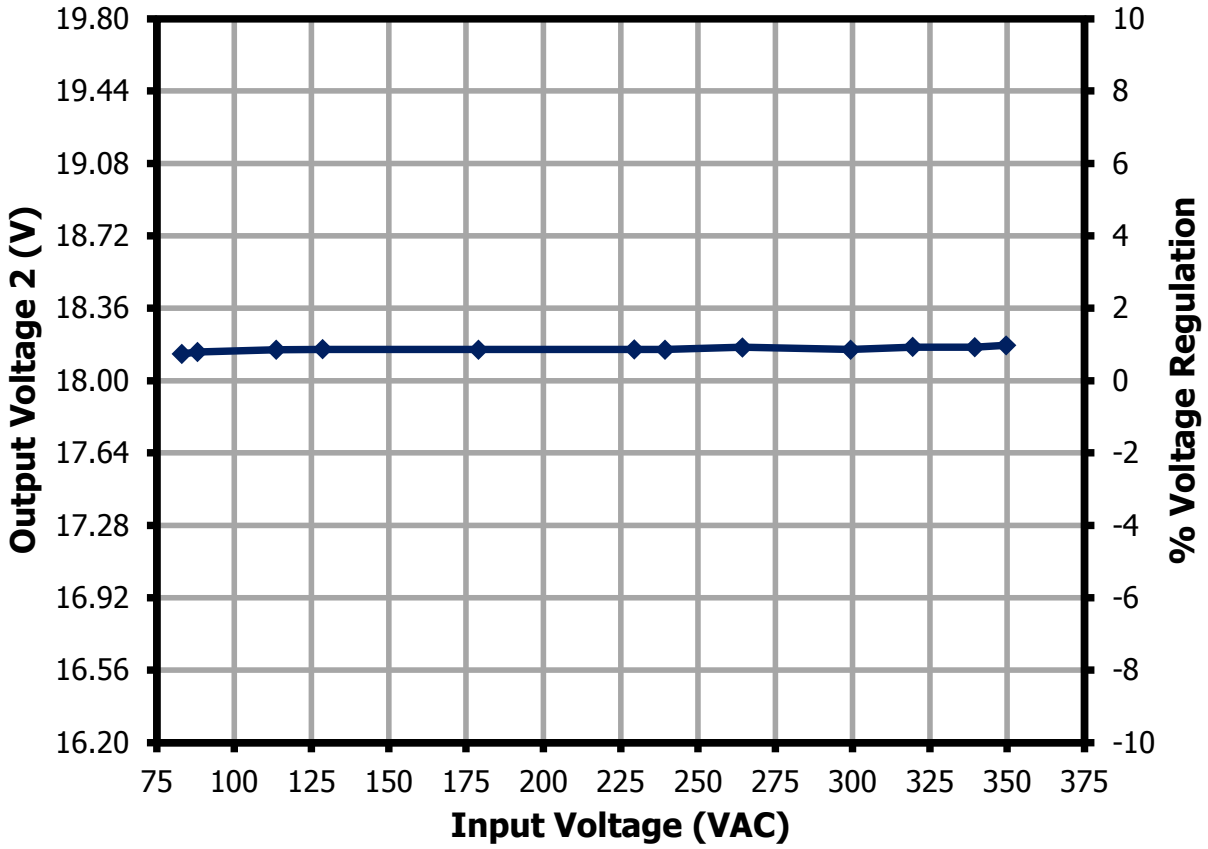


Figure 18 – 18 V_{OUT2} Output Regulation vs. Input Line Voltage.

10 Waveforms

10.1 Output Voltage Ripple

10.1.1 *Ripple Measurement Technique*

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 µF / 50 V ceramic type and one (1) 47 µF / 50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below). Ripple measurement was done at the end of the PCB.

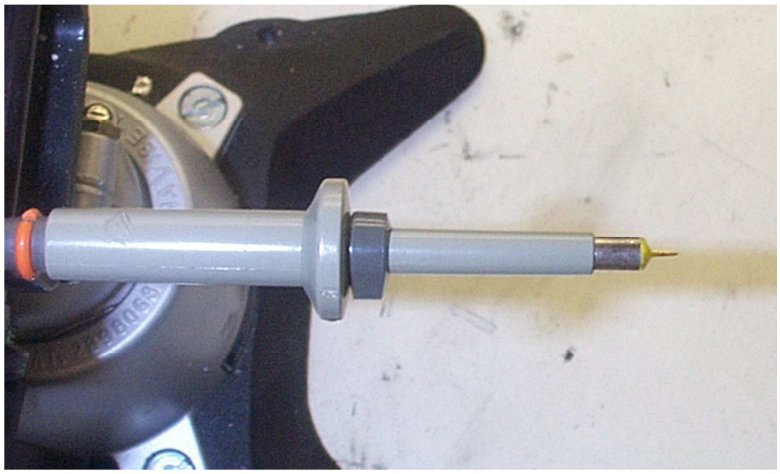


Figure 19 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed.)

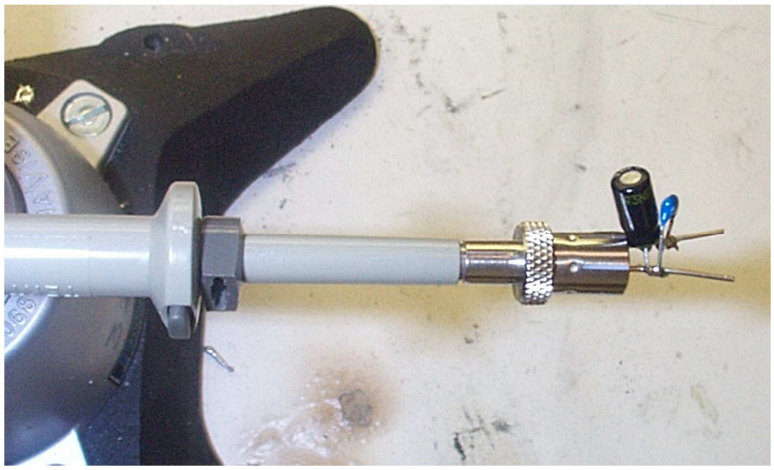


Figure 20 – Oscilloscope Probe with Probe Master (www.probemaster.com) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added.)

10.1.2 *Ripple Waveforms at Full Load*

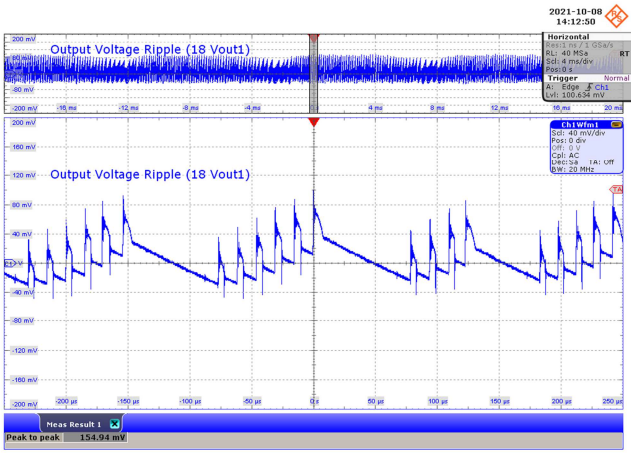


Figure 21 – 85 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 154.94 $mV_{PK-PK.}$

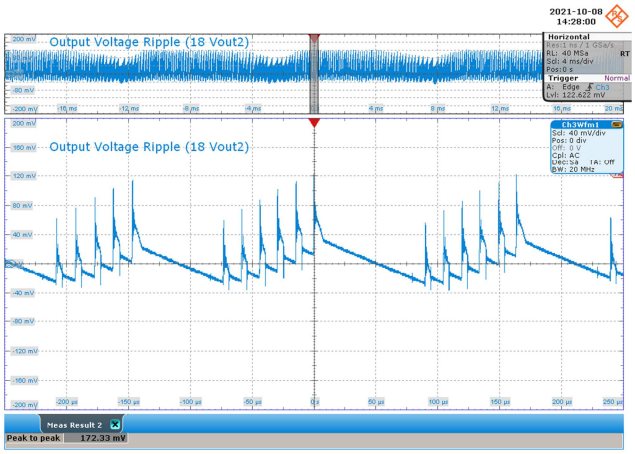


Figure 22 – 85 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 172.33 $mV_{PK-PK.}$

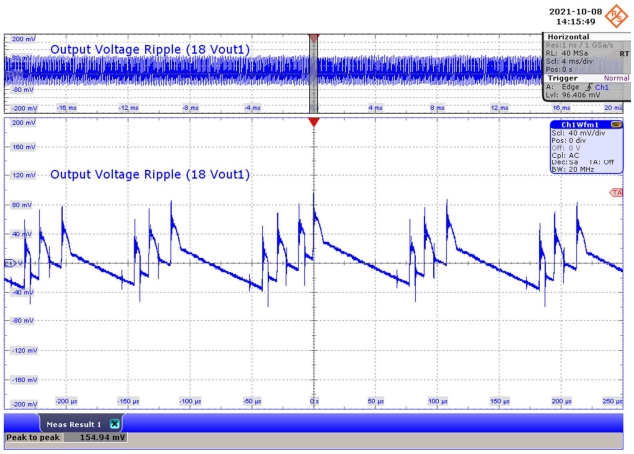


Figure 23 – 115 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 154.94 $mV_{PK-PK.}$

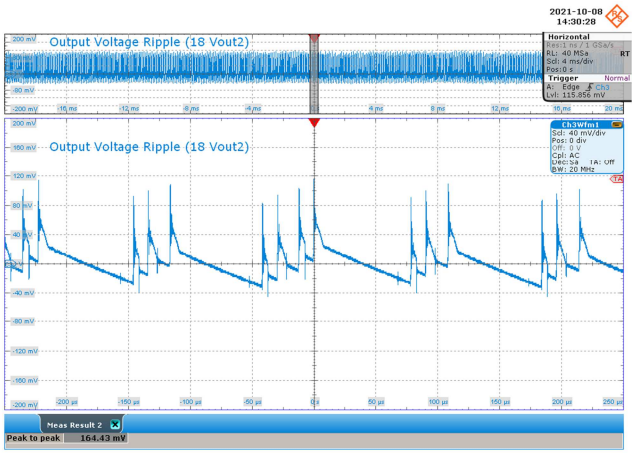


Figure 24 – 115 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 164.43 $mV_{PK-PK.}$

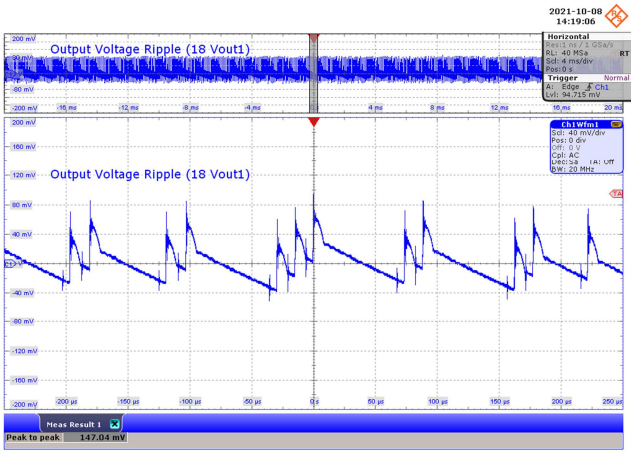


Figure 25 – 230 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 147.04 mV_{PK-PK}.

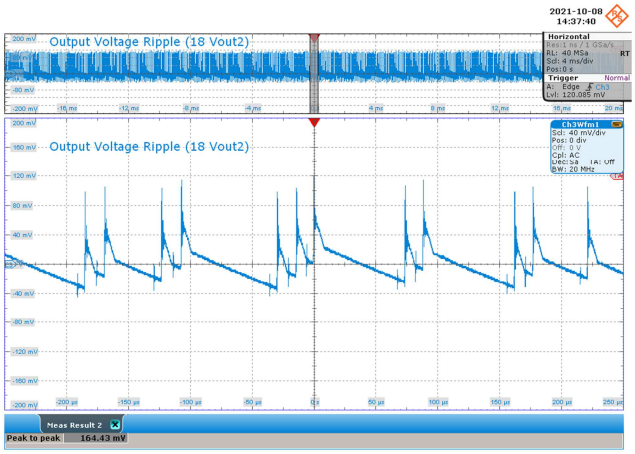


Figure 26 – 230 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 164.43 mV_{PK-PK}.

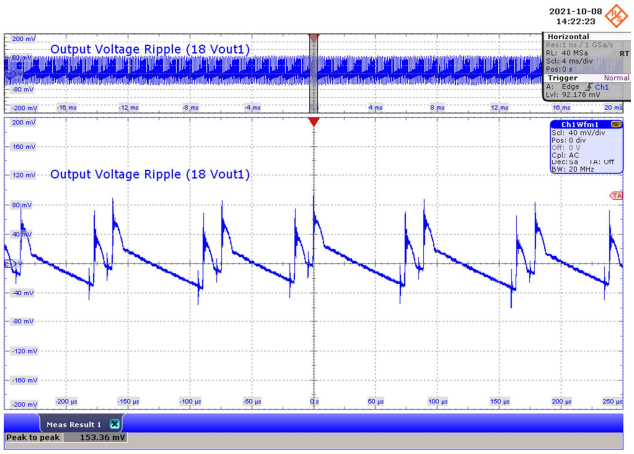


Figure 27 – 350 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 153.36 mV_{PK-PK}.

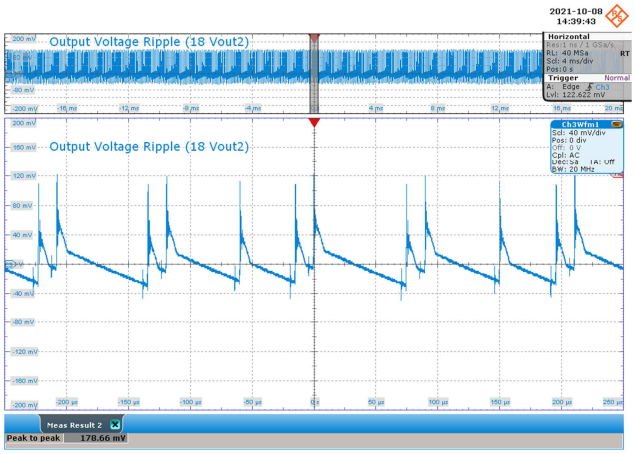


Figure 28 – 350 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 178.66 mV_{PK-PK}.

10.1.3 *Ripple Waveforms at No-Load*

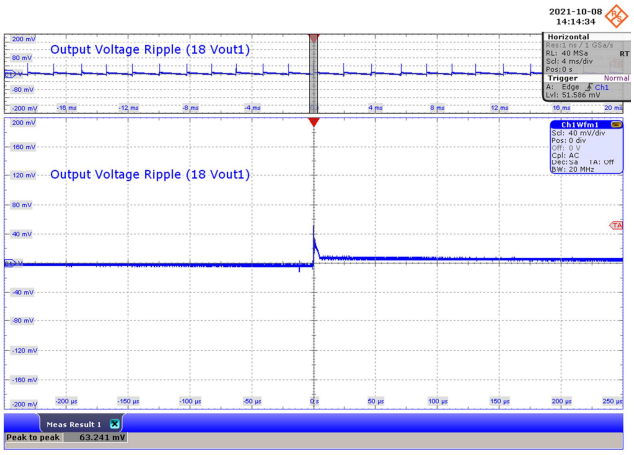


Figure 29 – 85 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 63.241 $mV_{PK-PK.}$

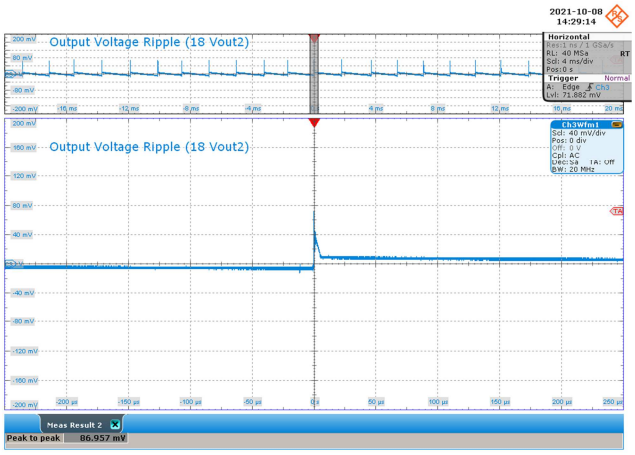


Figure 30 – 85 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 86.957 $mV_{PK-PK.}$

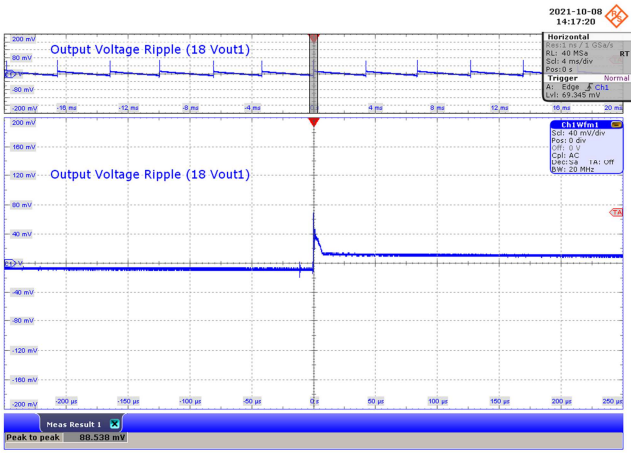


Figure 31 – 115 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 88.538 $mV_{PK-PK.}$

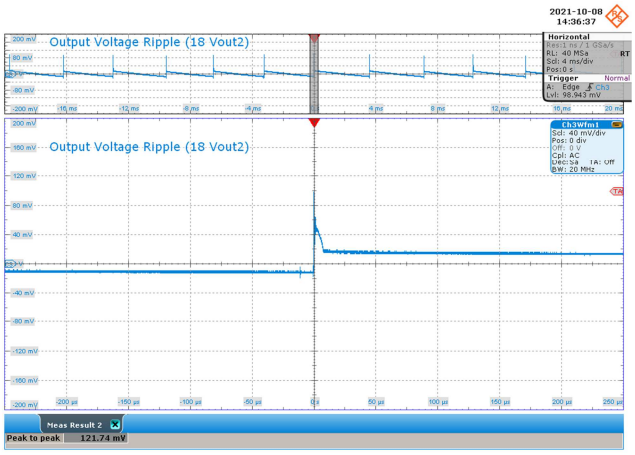


Figure 32 – 115 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 121.74 $mV_{PK-PK.}$

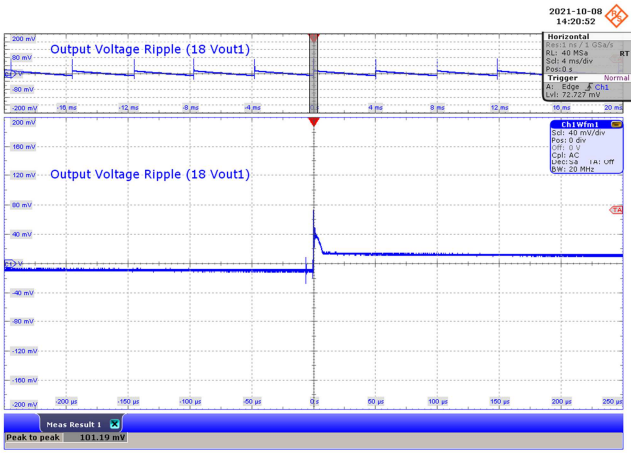


Figure 33 – 230 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 101.19 mV_{PK-PK}.

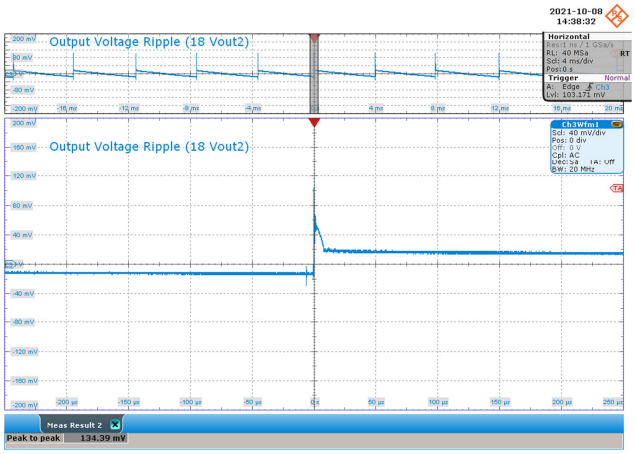


Figure 34 – 230 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 134.39 mV_{PK-PK}.

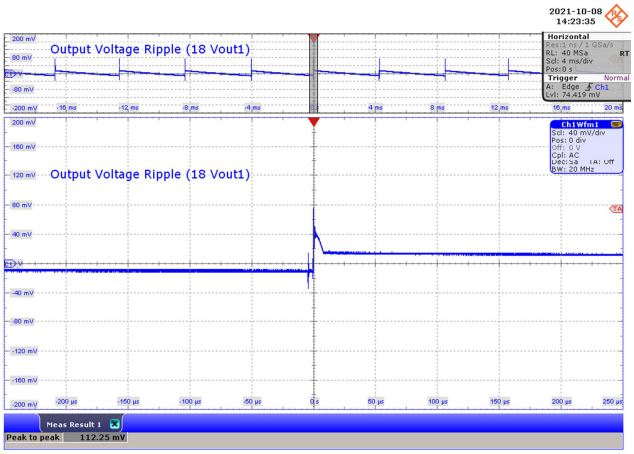


Figure 35 – 350 VAC Input. V_{OUT1} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT1} Ripple: 112.25 mV_{PK-PK}.

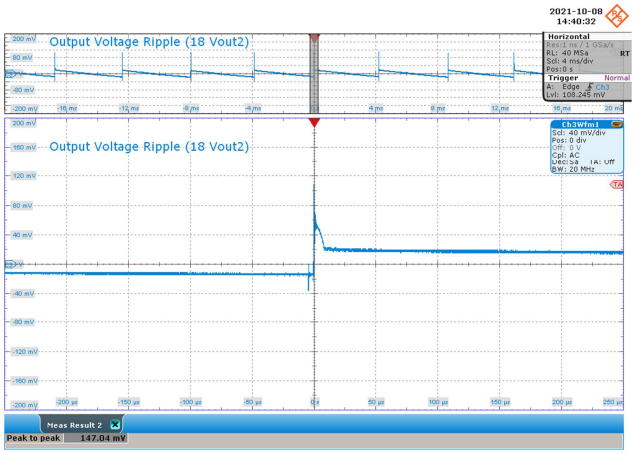


Figure 36 – 350 VAC Input. V_{OUT2} Ripple.
CH1: V_{RIPPLE}, 40 mV/ div., 4 ms / div.
Zoom: 50 µs / div.
18 V_{OUT2} Ripple: 147.04 mV_{PK-PK}.

10.1.4 *Ripple vs. Load*

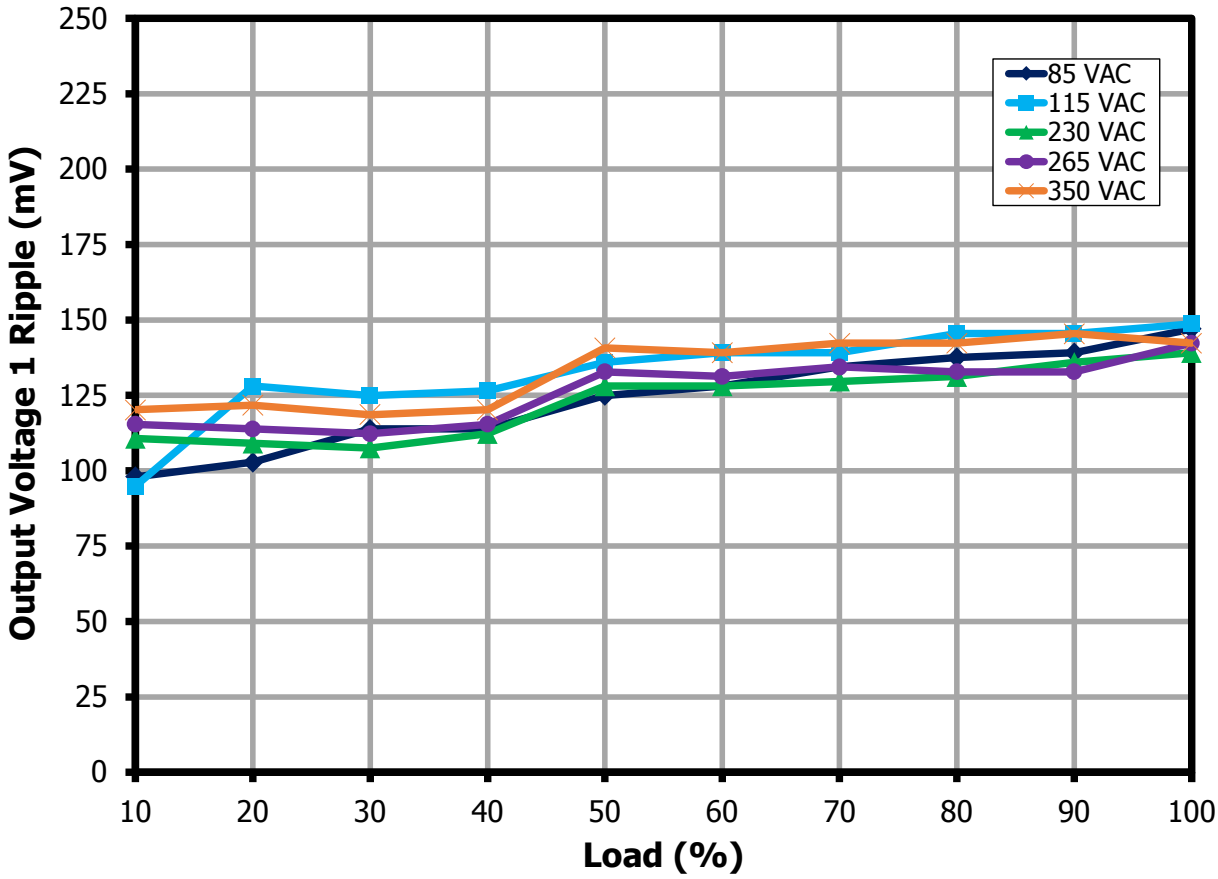


Figure 37 – 18 V_{OUT1} Output Ripple vs. Percent Load.

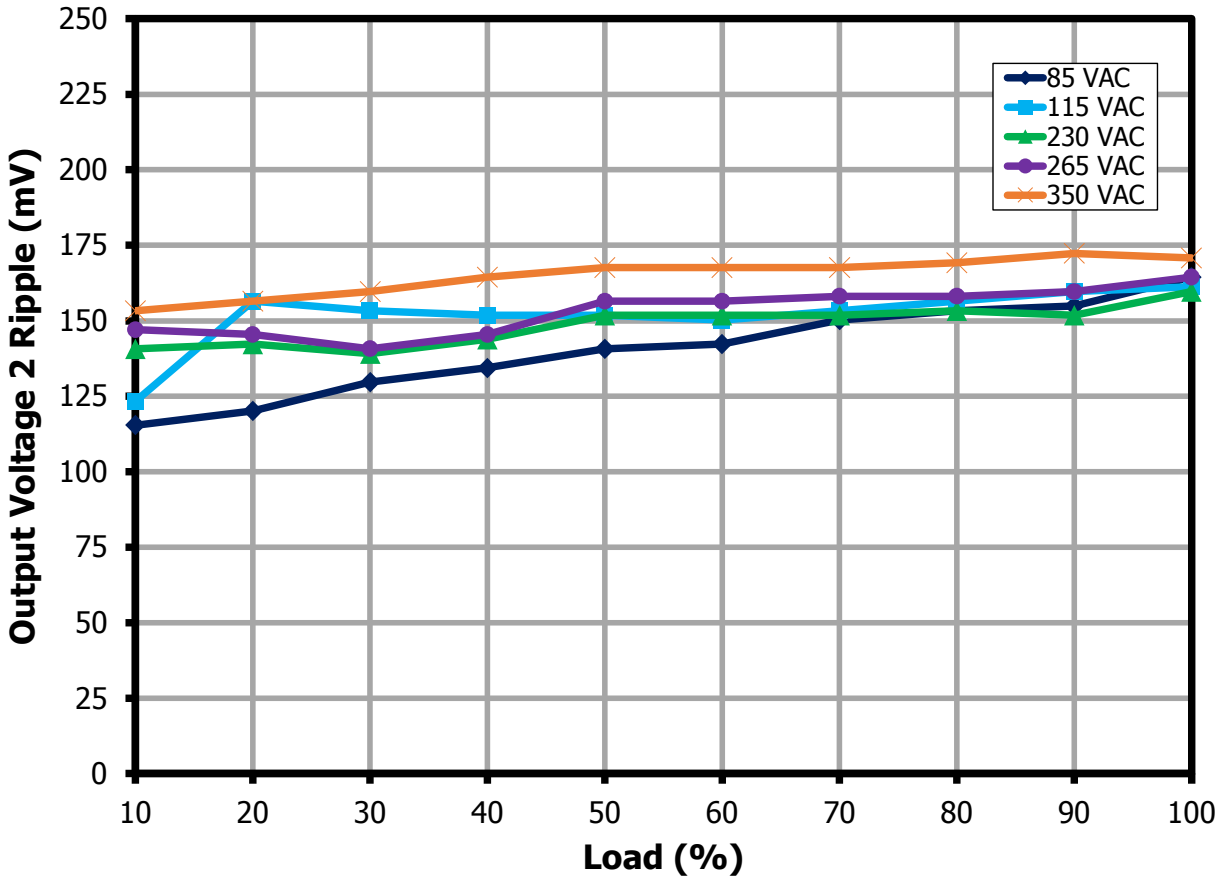


Figure 38 – 18 V_{OUT2} Output Ripple vs. Percent Load.

10.2 **Switching Waveforms**

10.2.1 *Drain Current and Drain Voltage*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

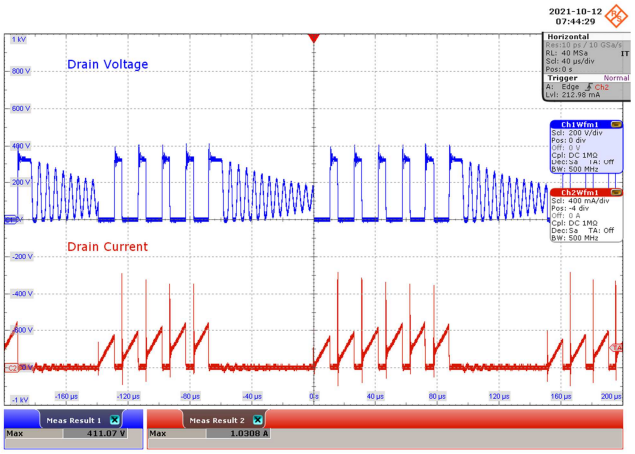


Figure 39 – 85 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 411.07 V.
$I_{DS(MAX)}$: 1.0308 A.

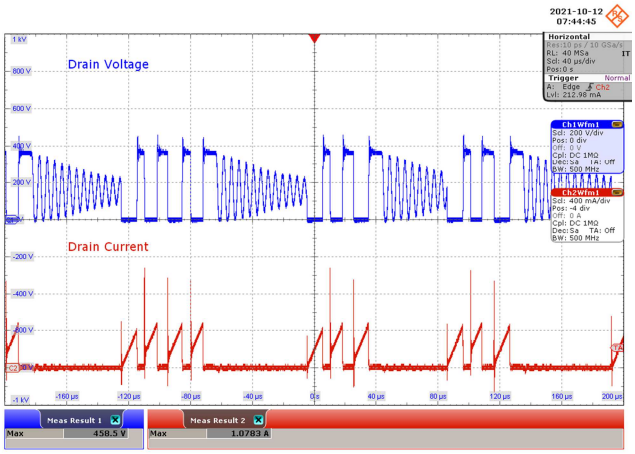


Figure 40 – 115 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 458.5 V.
$I_{DS(MAX)}$: 1.0783 A.

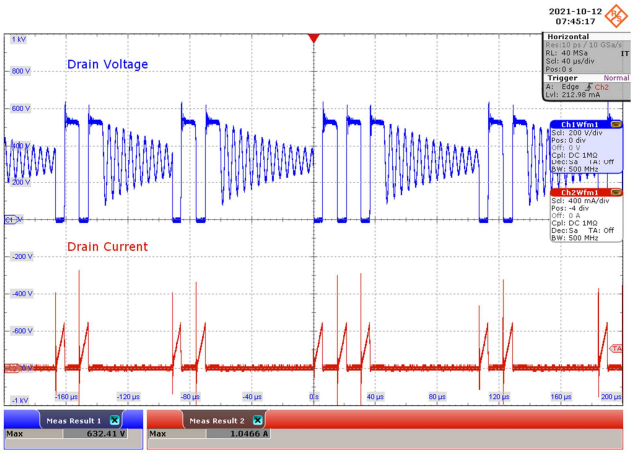


Figure 41 – 230 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 632.41 V.
$I_{DS(MAX)}$: 1.0466 A.

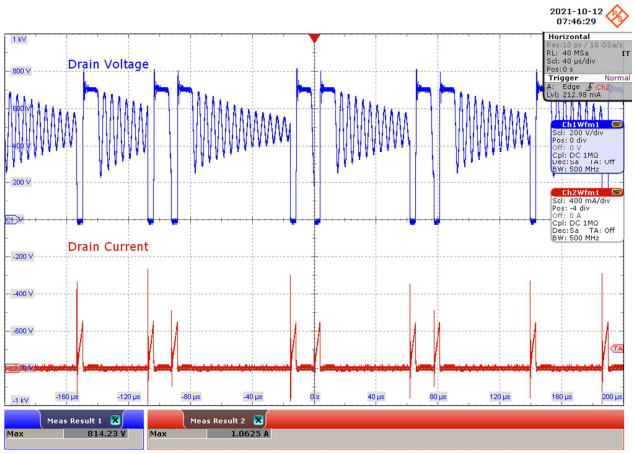


Figure 42 – 350 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 814.23 V.
$I_{DS(MAX)}$: 1.0625 mA.

10.2.2 *18 V_{OUT1} Output Diode Voltage and Current*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

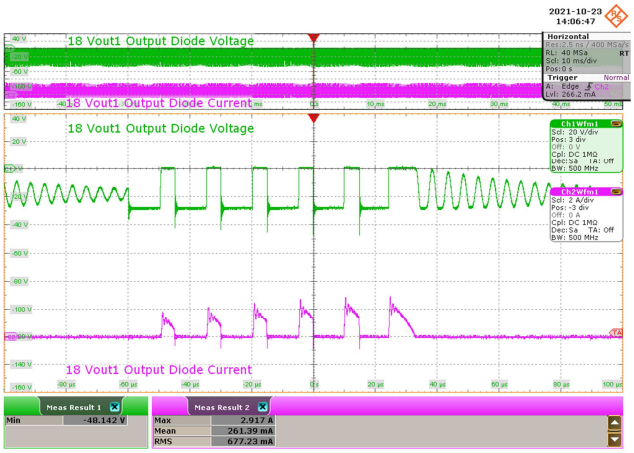


Figure 43 – 85 VAC Input.
CH1: Diode 1 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 1 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 48.142 V.
$I_{D(MEAN)}$: 261.39 mA.

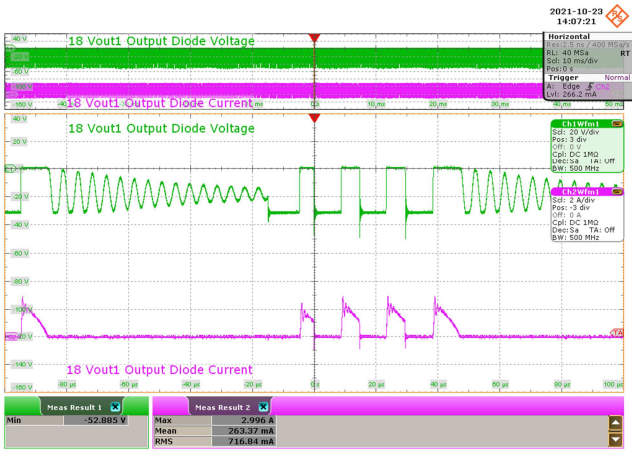


Figure 44 – 115 VAC Input.
CH1: Diode 1 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 1 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 52.885 V.
$I_{D(MEAN)}$: 263.37 mA.

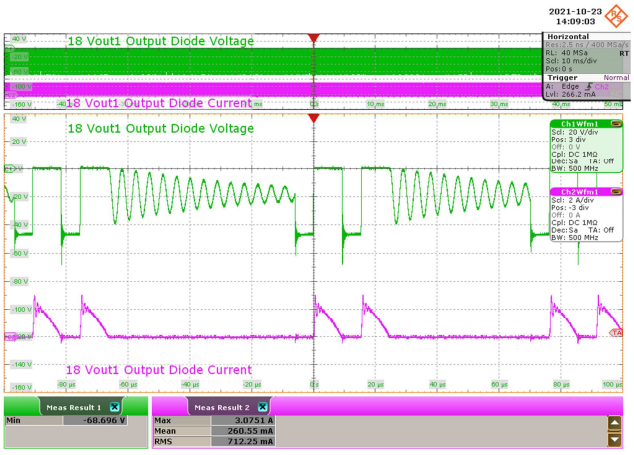


Figure 45 – 230 VAC Input.
CH1: Diode 1 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 1 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 68.696 V.
$I_{D(MEAN)}$: 260.55 mA.

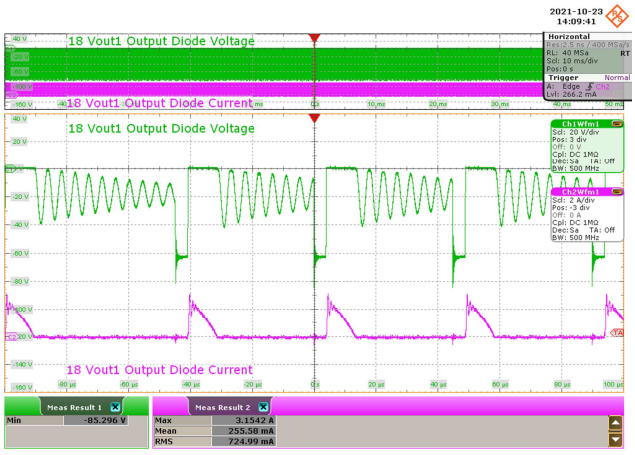


Figure 46 – 350 VAC Input.
CH1: Diode 1 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 1 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 85.296 V.
$I_{D(MEAN)}$: 255.58 mA.

10.2.3 *18 V_{OUT2} Output Diode Voltage and Current*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

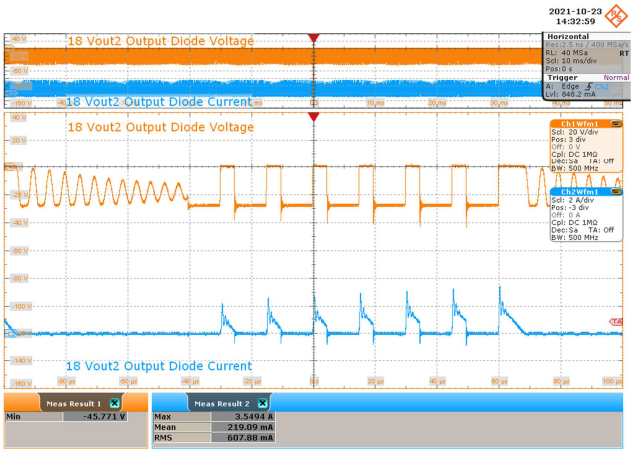


Figure 47 – 85 VAC Input.
CH1: Diode 2 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 2 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 45.771 V.
$I_{D(MEAN)}$: 219.09 mA.

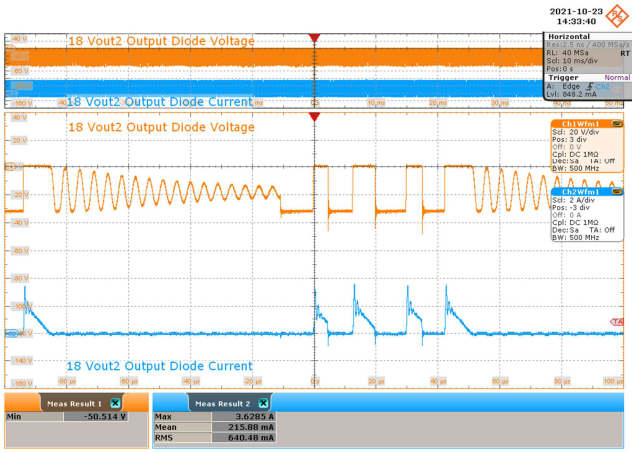


Figure 48 – 115 VAC Input.
CH1: Diode 2 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 2 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 50.514 V.
$I_{D(MEAN)}$: 215.88 mA.

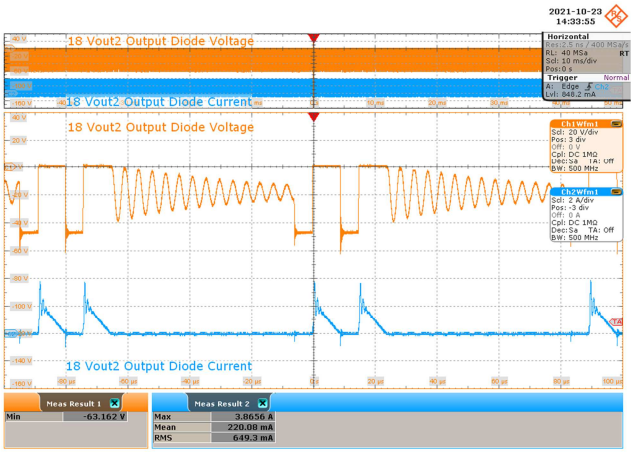


Figure 49 – 230 VAC Input.
CH1: Diode 2 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 2 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 63.162 V.
$I_{D(MEAN)}$: 220.08 mA.

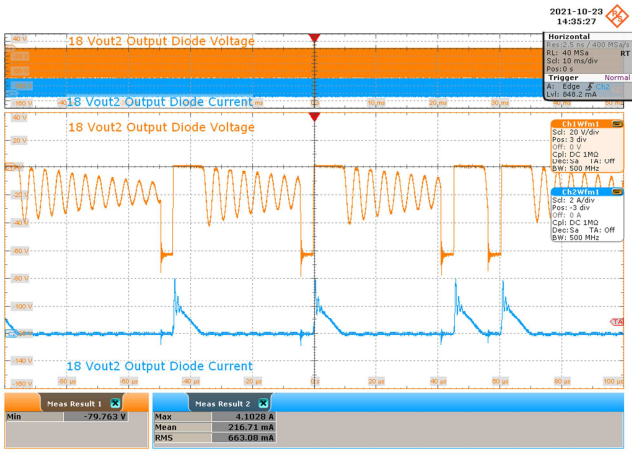


Figure 50 – 350 VAC Input.
CH1: Diode 2 Voltage, 20 V / div., 10 ms / div.
CH2: Diode 2 Current, 2 A / div., 10 ms / div.
Zoom: 20 µs / div.
PIV: 79.763 V.
$I_{D(MEAN)}$: 216.71 mA.

10.3 **Start-up Performance**

10.3.1 *18 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CC Load*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

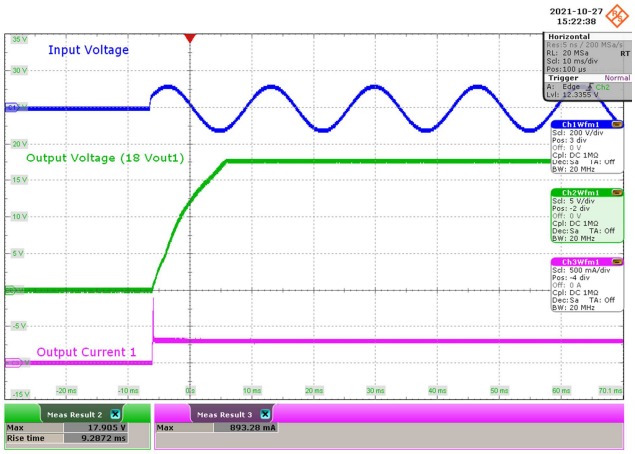


Figure 51 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 9.2872 ms.

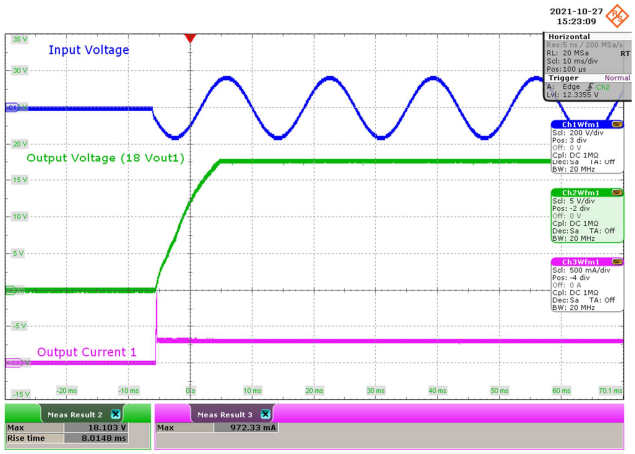


Figure 52 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 8.0148 ms.

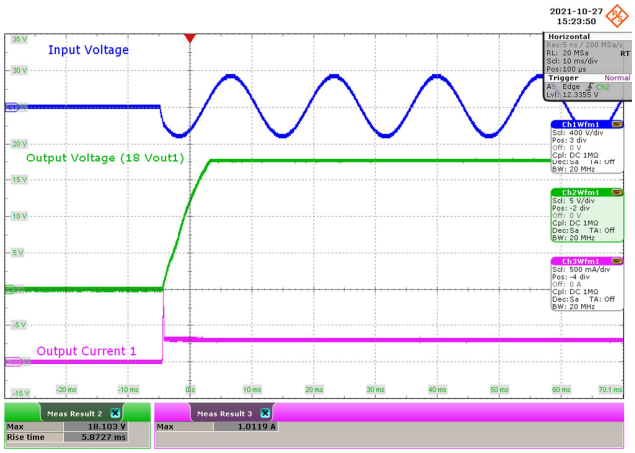


Figure 53 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 5.8727 ms.

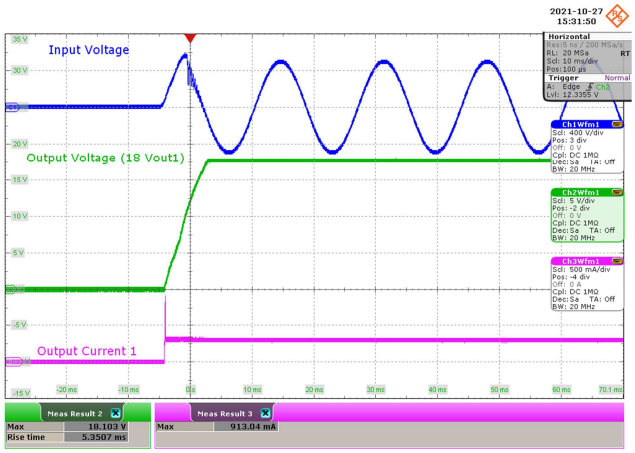


Figure 54 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 5.3507 ms.

10.3.2 *18 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CR Load*

Test conditions: 18 V_{OUT1} load set to CR at 60 Ω, 18 V_{OUT2} load set to CR at 72 Ω

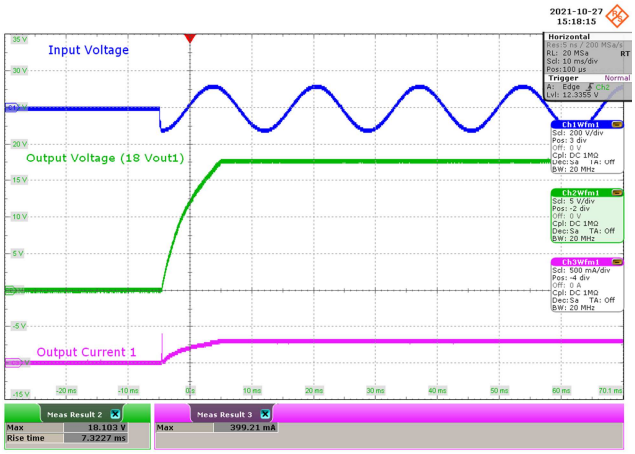


Figure 55 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 7.3227 ms.

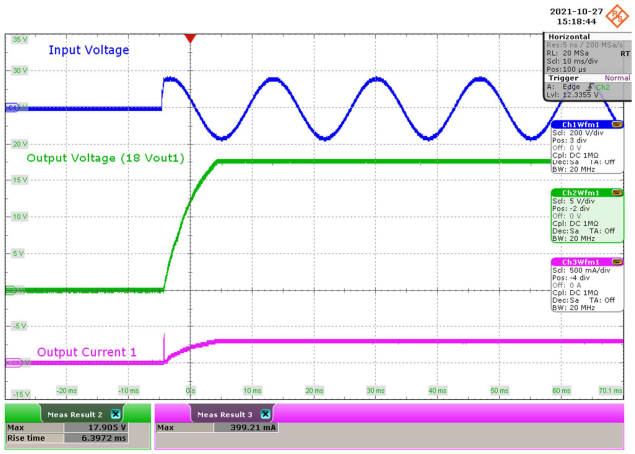


Figure 56 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 6.3972 ms.

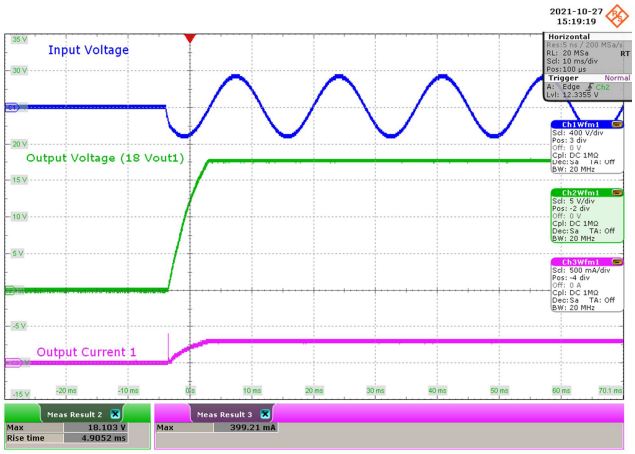


Figure 57 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 4.9052 ms.

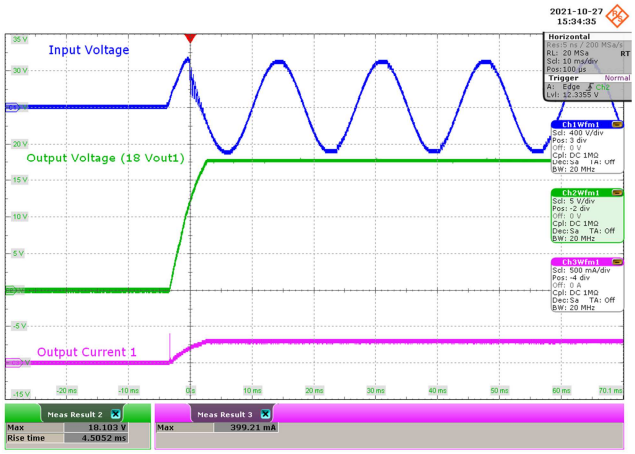


Figure 58 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 4.5052 ms.

10.3.3 *18 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CC Load*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

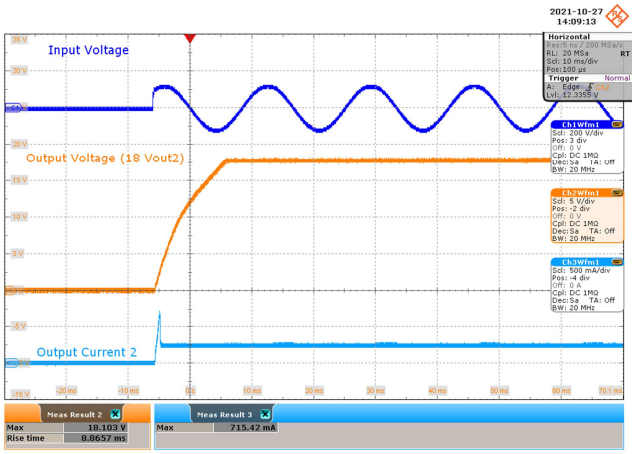


Figure 59 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 8.8657 ms.

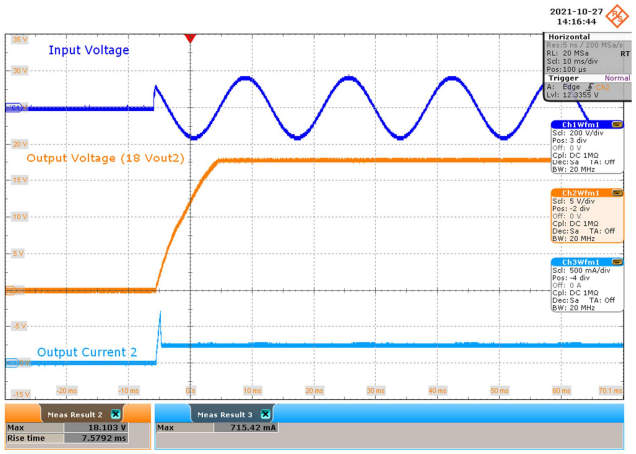


Figure 60 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 7.5792 ms.

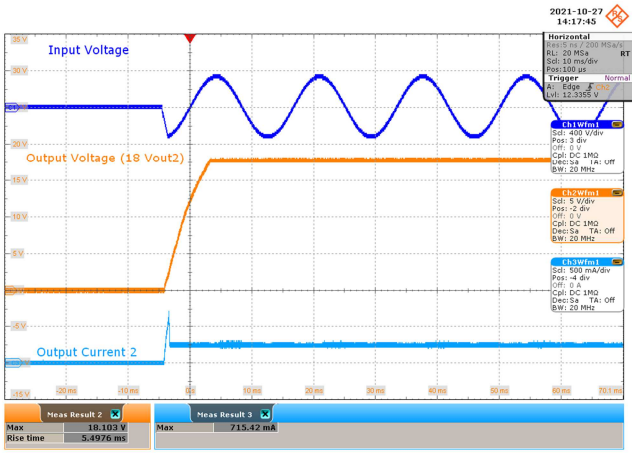


Figure 61 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 5.4976 ms.

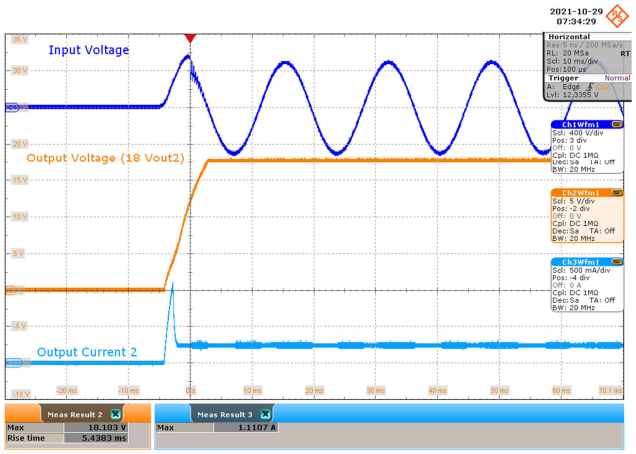


Figure 62 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 5.4383 ms.

10.3.4 *18 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CR Load*

Test conditions: 18 V_{OUT1} load set to CR at 60 Ω, 18 V_{OUT2} load set to CR at 72 Ω

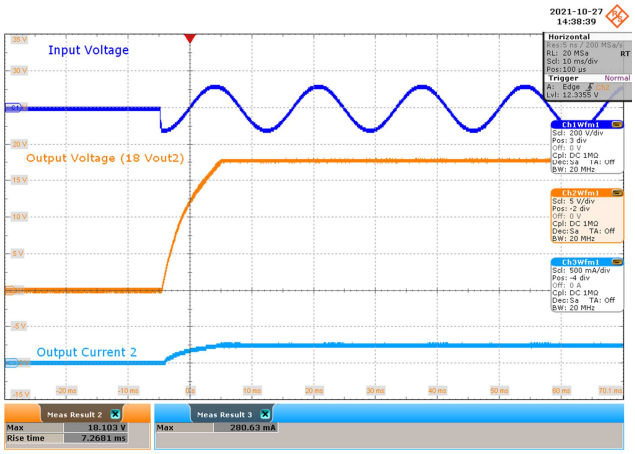


Figure 63 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 7.2681 ms.

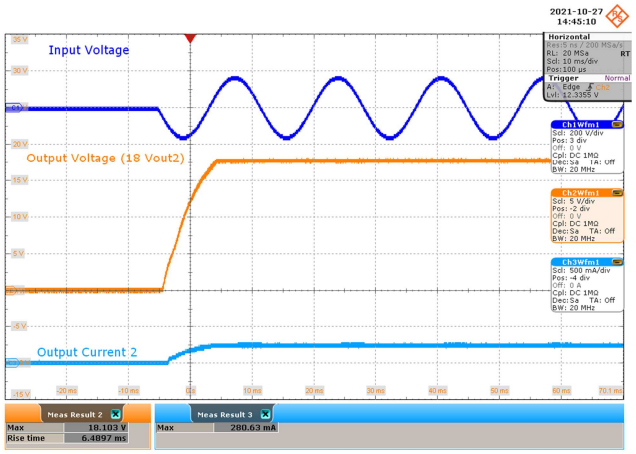


Figure 64 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 6.4897 ms.

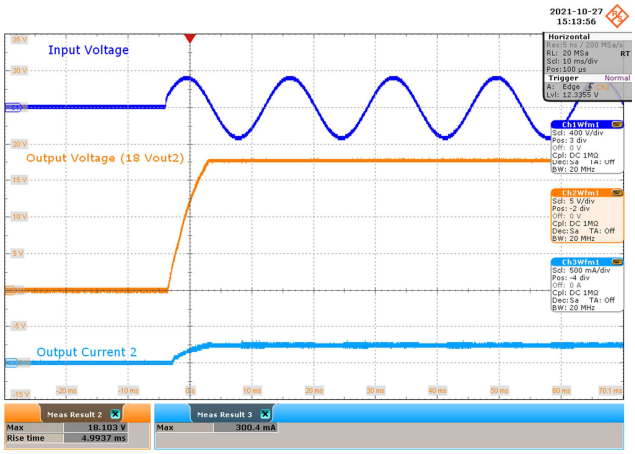


Figure 65 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 4.9937 ms.

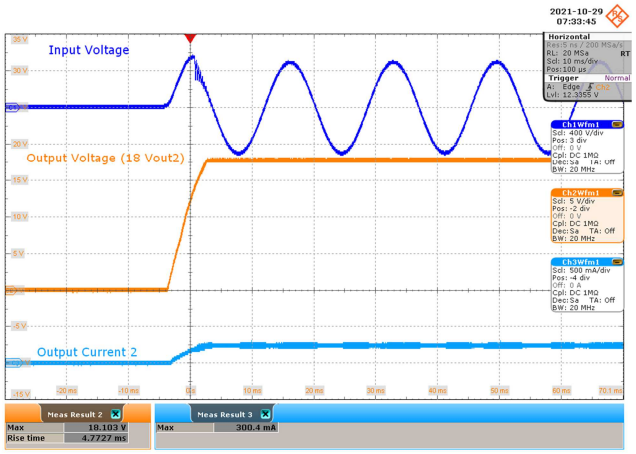


Figure 66 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 4.7727 ms.

10.3.5 *Drain Current and Drain Voltage Start-up Operation*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

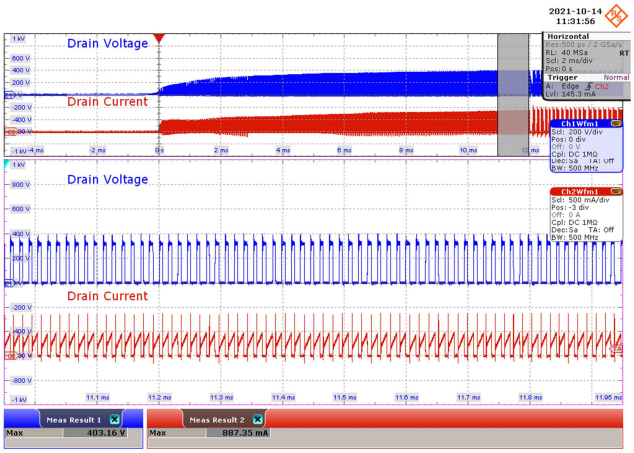


Figure 67 – 85 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 403.16 V.
$I_{DS(MAX)}$: 0.88735 A.

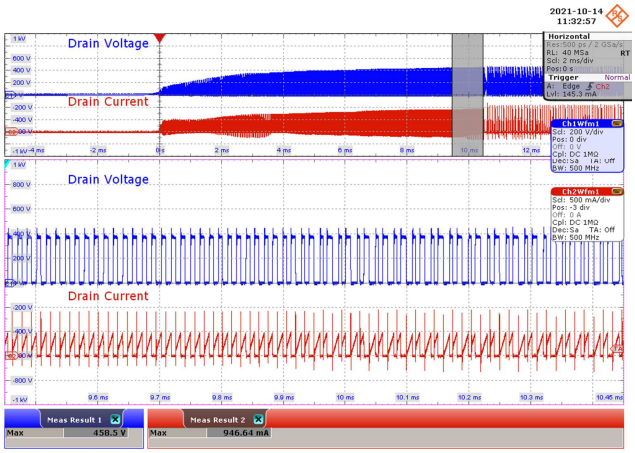


Figure 68 – 115 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 458.5 V.
$I_{DS(MAX)}$: 0.94664 A.

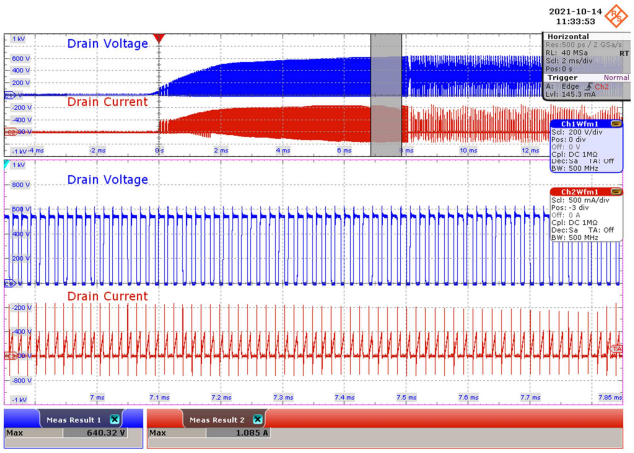


Figure 69 – 230 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 640.32 V.
$I_{DS(MAX)}$: 1.085 A.

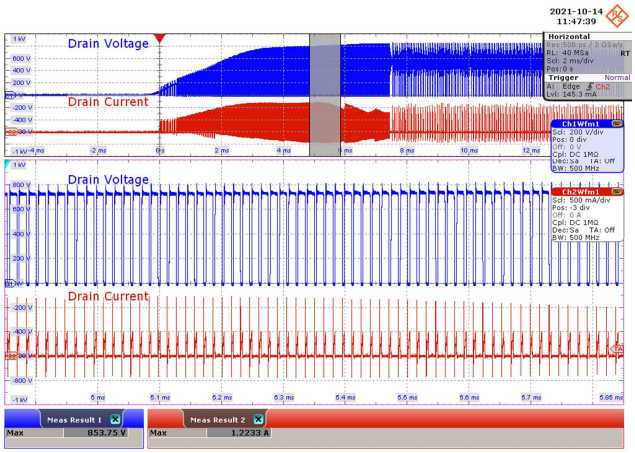


Figure 70 – 350 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 853.75 V.
$I_{DS(MAX)}$: 1.2233 A.

10.4 **Output Load Transient**

10.4.1 *18 V_{OUT1} Output Transient*

Test conditions: 18 V_{OUT1} load swings from 30 mA to full load, 18 V_{OUT2} at full load. Output current was set at dynamic loading conditions of 100 Hz frequency at 50% duty. Slew rate of 0.5 A / µs was used.

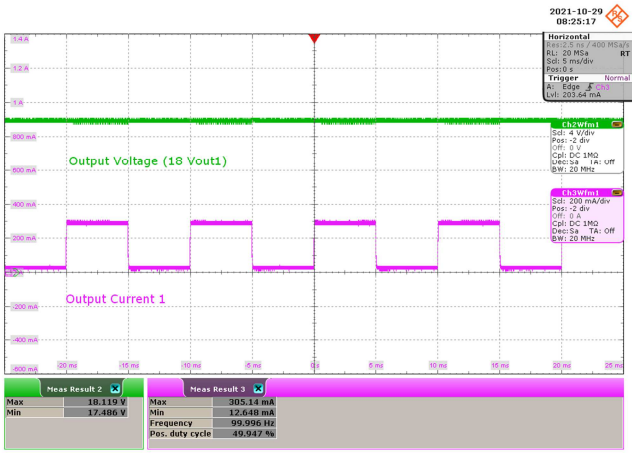


Figure 71 – 85 VAC Input.
CH2: Output Voltage 1, 4 V / div., 5 ms / div.
CH3: Output Current 1, 200 mA / div., 5 ms / div.
V_{MAX}: 18.119 V.
V_{MIN}: 17.486 V.

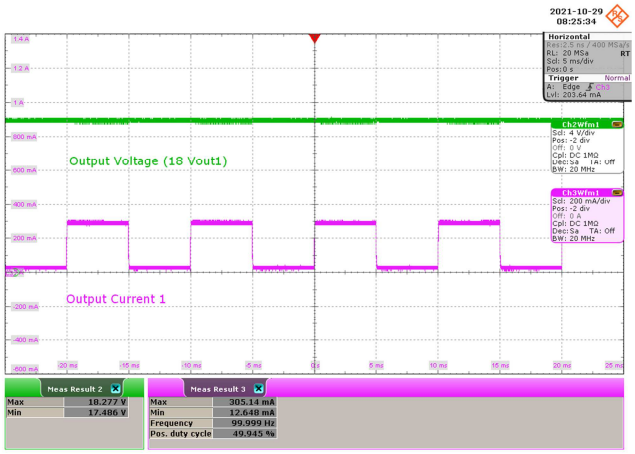


Figure 72 – 115 VAC Input.
CH2: Output Voltage 1, 4 V / div., 5 ms / div.
CH3: Output Current 1, 200 mA / div., 5 ms / div.
V_{MAX}: 18.277 V.
V_{MIN}: 17.486 V.

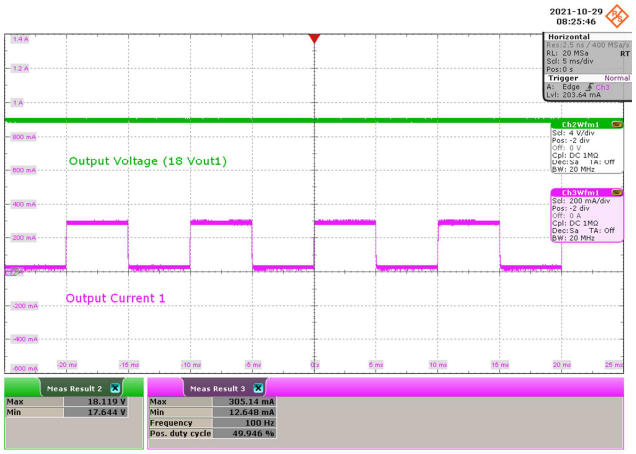


Figure 73 – 230 VAC Input.
CH2: Output Voltage 1, 4 V / div., 5 ms / div.
CH3: Output Current 1, 200 mA / div., 5 ms / div.
V_{MAX}: 18.119 V.
V_{MIN}: 17.644 V.

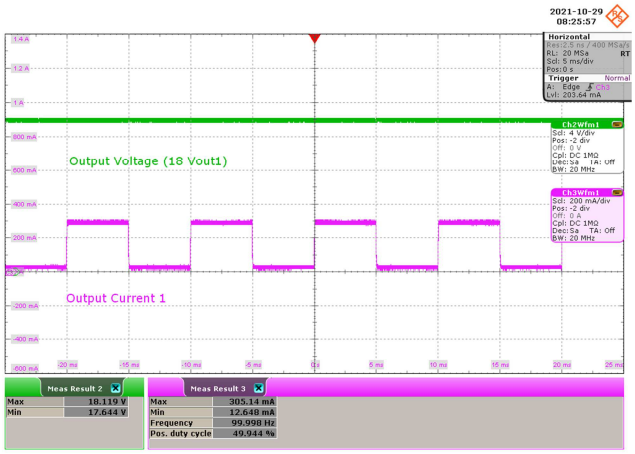


Figure 74 – 350 VAC Input.
CH2: Output Voltage 1, 4 V / div., 5 ms / div.
CH3: Output Current 1, 200 mA / div., 5 ms / div.
V_{MAX}: 18.119 V.
V_{MIN}: 17.644 V.

10.4.2 *18 V_{OUT2} Output Transient*

Test conditions: 18 V_{OUT2} load swings from 25 mA to full load, 18 V_{OUT1} at full load. Output current was set at dynamic loading conditions of 100 Hz frequency at 50% duty. Slew rate of 0.5 A / µs was used.

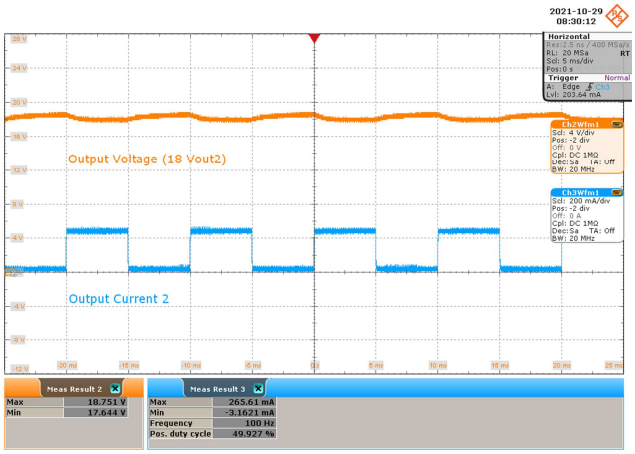


Figure 75 – 85 VAC Input.
CH2: Output Voltage 2, 4 V / div., 5 ms / div.
CH3: Output Current 2, 200 mA / div., 5 ms / div.
V_{MAX}: 18.751 V.
V_{MIN}: 17.644 V.

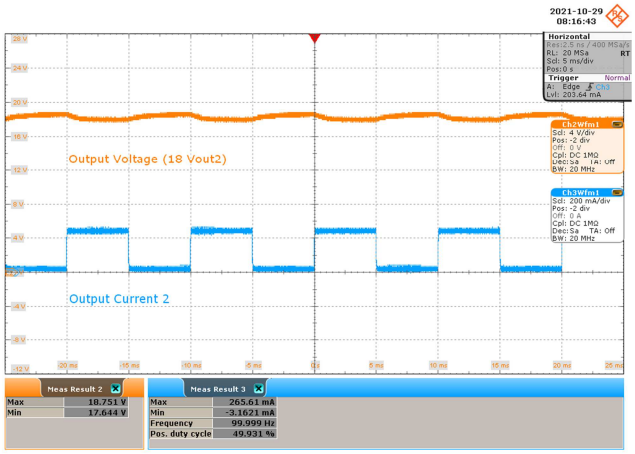


Figure 76 – 115 VAC Input.
CH2: Output Voltage 2, 4 V / div., 5 ms / div.
CH3: Output Current 2, 200 mA / div., 5 ms / div.
V_{MAX}: 18.751 V.
V_{MIN}: 17.644 V.

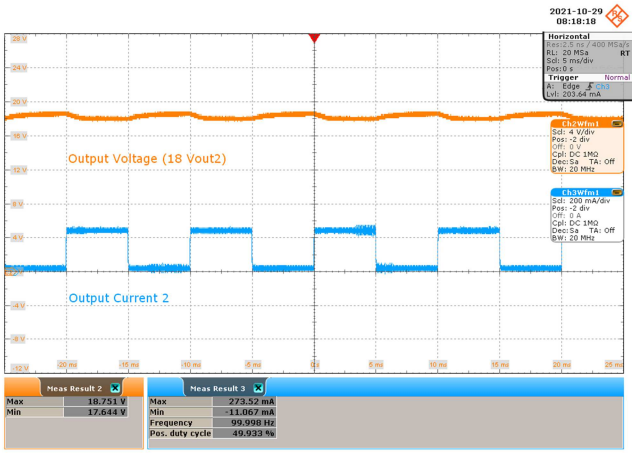


Figure 77 – 230 VAC Input.
CH2: Output Voltage 2, 4 V / div., 5 ms / div.
CH3: Output Current 2, 200 mA / div., 5 ms / div.
V_{MAX}: 18.751 V.
V_{MIN}: 17.644 V.

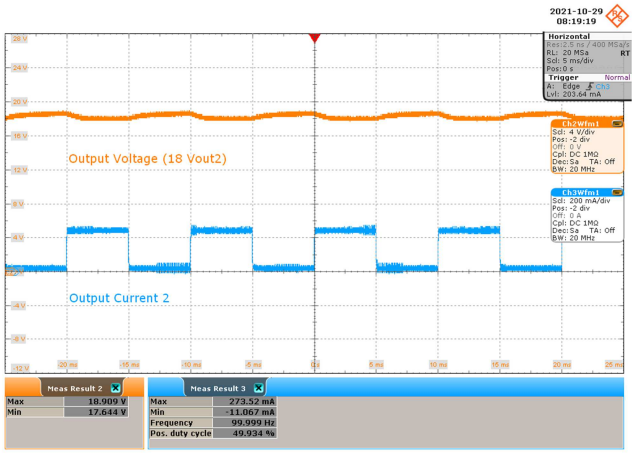


Figure 78 – 350 VAC Input.
CH2: Output Voltage 2, 4 V / div., 5 ms / div.
CH3: Output Current 2, 200 mA / div., 5 ms / div.
V_{MAX}: 18.909 V.
V_{MIN}: 17.644 V.

10.5 **Fault Waveforms**

10.5.1 *18 V_{OUT1} Output Short*

Test conditions: Both outputs at full load before short.

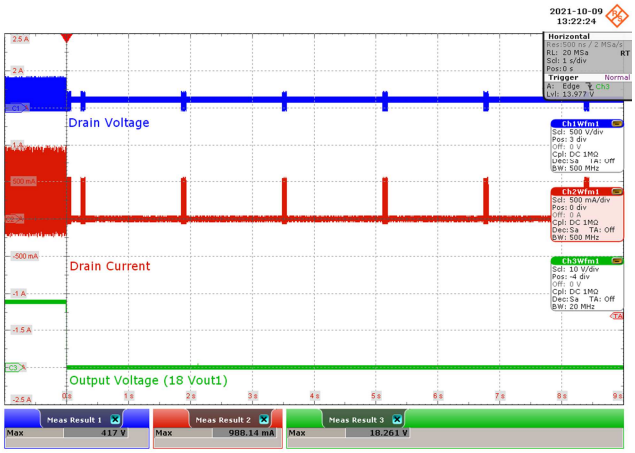


Figure 79 – 85 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 1, 10 V / div., 1 s / div.

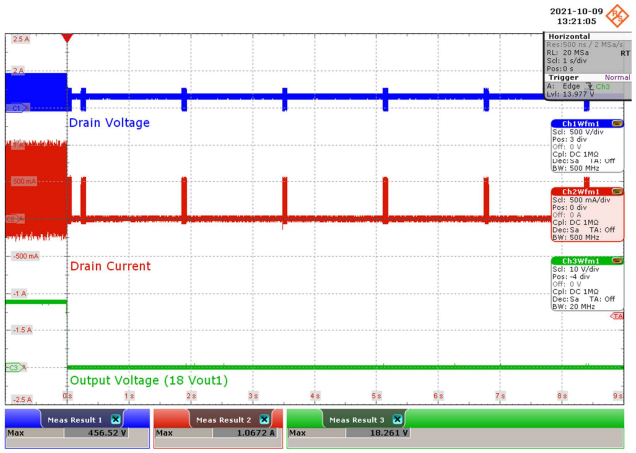


Figure 80 – 115 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 1, 10 V / div., 1 s / div.

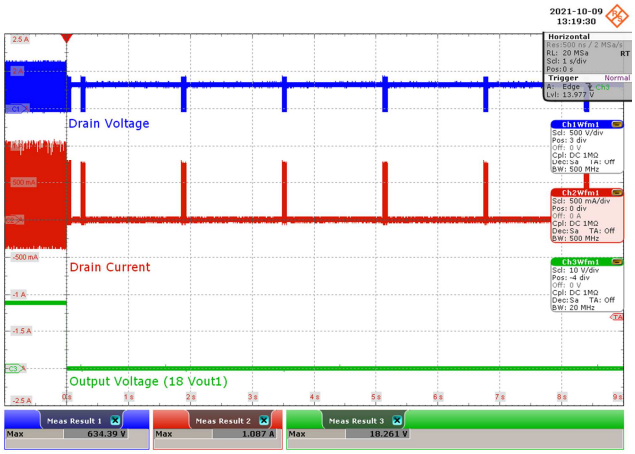


Figure 81 – 230 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 1, 10 V / div., 1 s / div.

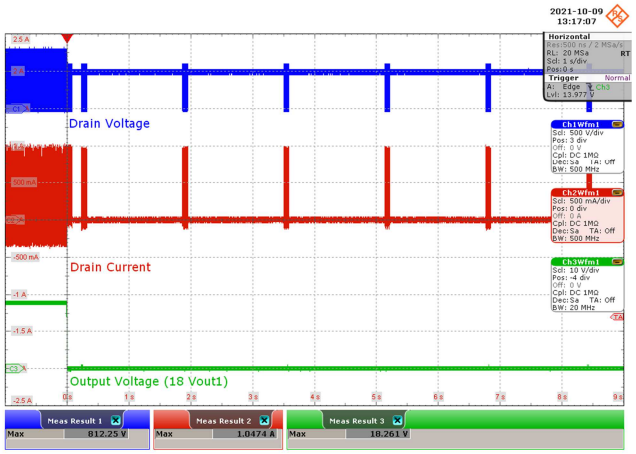


Figure 82 – 350 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 1, 10 V / div., 1 s / div.

10.5.2 *18 V_{OUT2} Output Short*

Test conditions: Both outputs at full load before short.

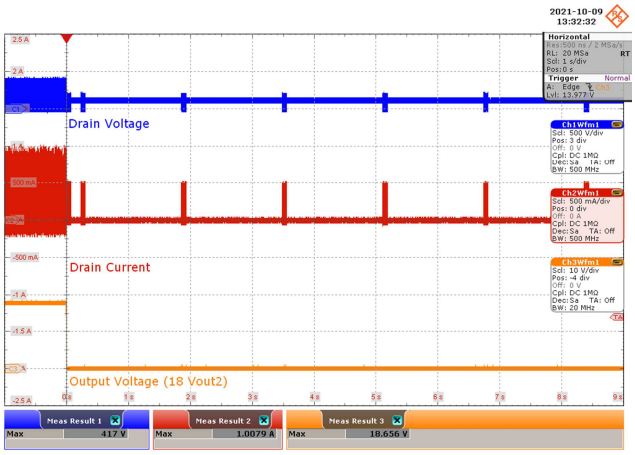


Figure 83 – 85 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 2, 10 V / div., 1 s / div.

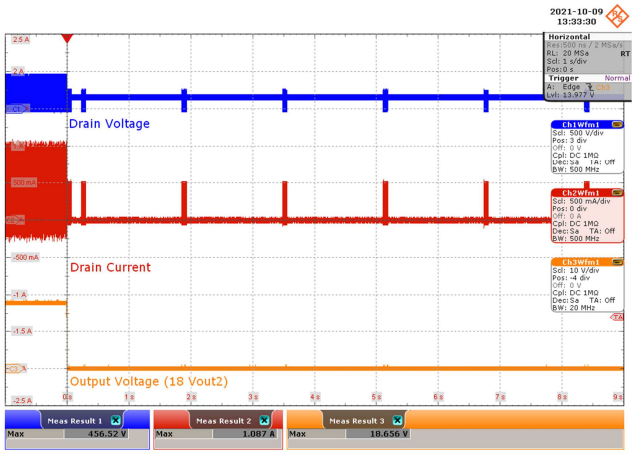


Figure 84 – 115 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 2, 10 V / div., 1 s / div.

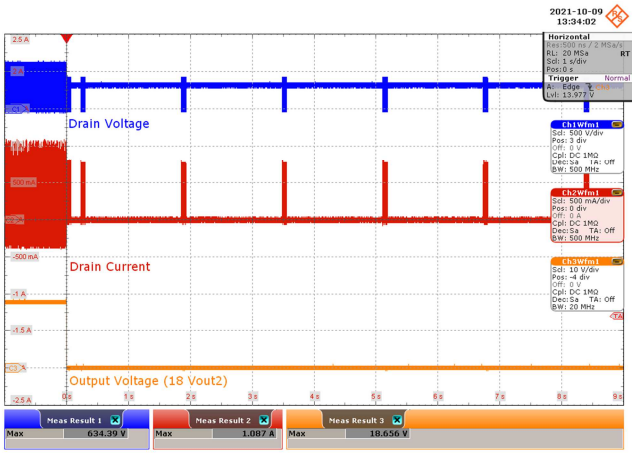


Figure 85 – 230 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 2, 10 V / div., 1 s / div.

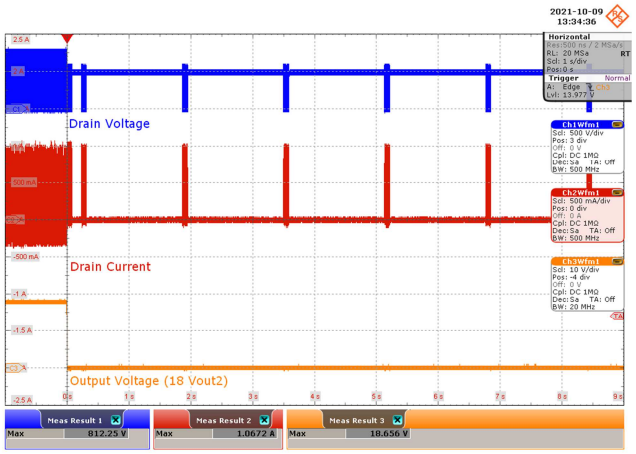


Figure 86 – 350 VAC Input.
CH1: Drain Voltage, 500 V / div., 1 s / div.
CH2: Drain Current, 500 mA / div., 1 s / div.
CH3: Output Voltage 2, 10 V / div., 1 s / div.

11 Thermal Performance

11.1 Test Set-Up

Thermal evaluation was performed under two conditions: (1) room temperature with the circuit board enclosed inside an acrylic box and (2), 50 ºC ambient inside a thermal chamber. In both conditions, the circuit is soaked for one hour under full load conditions.

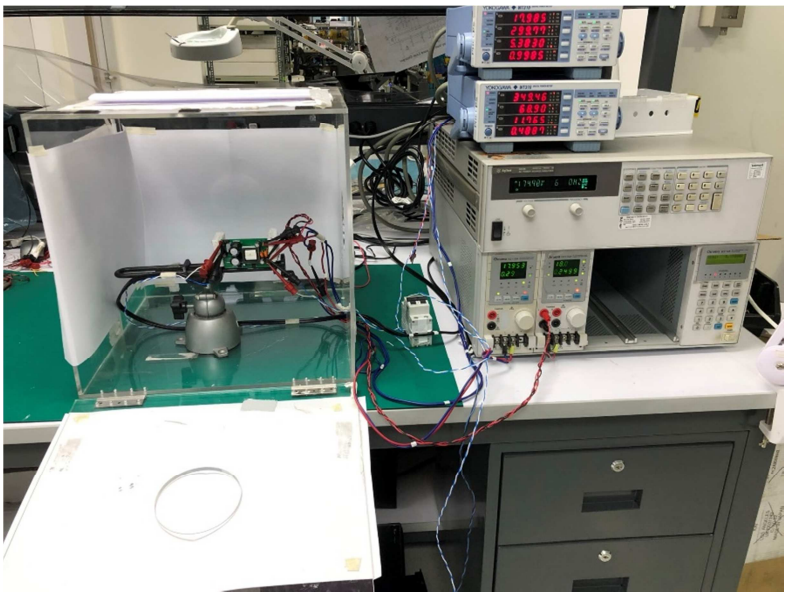


Figure 87 – Thermal Performance Set-up Using an Acrylic Box.

Figure 88 – Thermal Performance Set-up Using Thermal Chamber.

11.2 **Room Temperature**

11.2.1 *85 VAC, Room Temperature*

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	18 V_{OUT1} Output Diode (D3)	18 V_{OUT2} Output Diode (D4)	Ambient Temperature
62.6 ºC	51.0 ºC	45.5 ºC	52.9 ºC	53.1 ºC	50.6 ºC	24.5 ºC

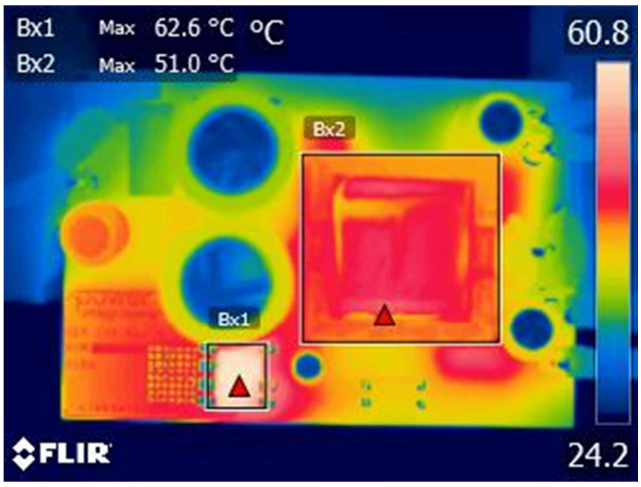


Figure 89 – Ambient = 24.2 ºC.
Bx1, U1: 62.6 ºC.
Bx2, T1: 51.0 ºC.

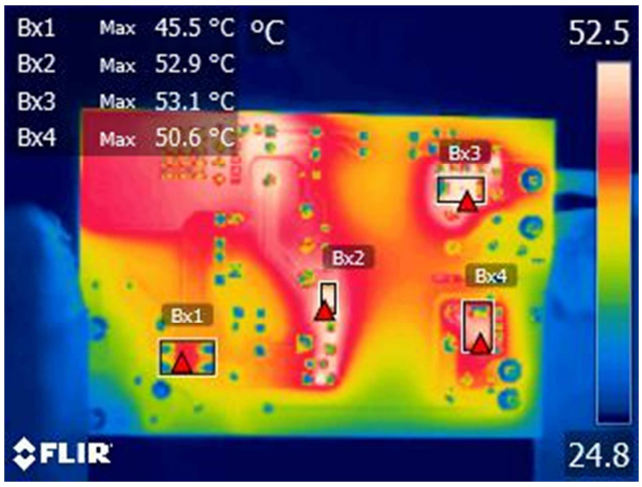


Figure 90 – Ambient = 24.8 ºC.
Bx1, BR1: 45.5 ºC.
Bx2, D1: 52.9 ºC.
Bx3, D3: 53.1 ºC.
Bx4, D4: 50.6 ºC.

11.2.2 *350 VAC, Room Temperature*

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	18 V_{OUT1} Output Diode (D3)	18 V_{OUT2} Output Diode (D4)	Ambient Temperature
45.5 ºC	49.2 ºC	36.3 ºC	45.1 ºC	53.6 ºC	51.2 ºC	24.3 ºC

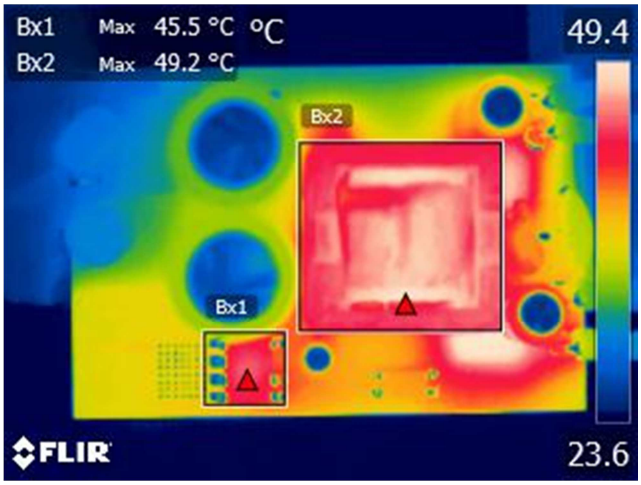


Figure 91 – Ambient = 23.6 ºC.
Bx1, U1: 45.5 ºC.
Bx2, T1: 49.2 ºC.

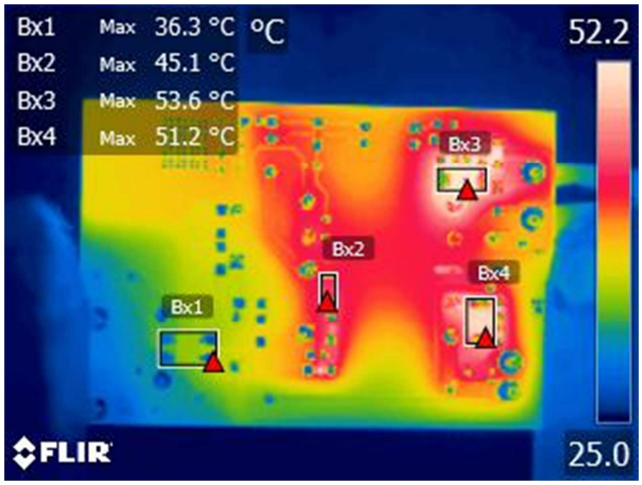


Figure 92 – Ambient = 25.0 ºC.
Bx1, BR1: 36.3 ºC.
Bx2, D1: 45.1 ºC.
Bx3, D3: 53.6 ºC.
Bx4, D4: 51.2 ºC.

11.3 **50 ºC Ambient**

11.3.1 *85 VAC, 50 ºC*

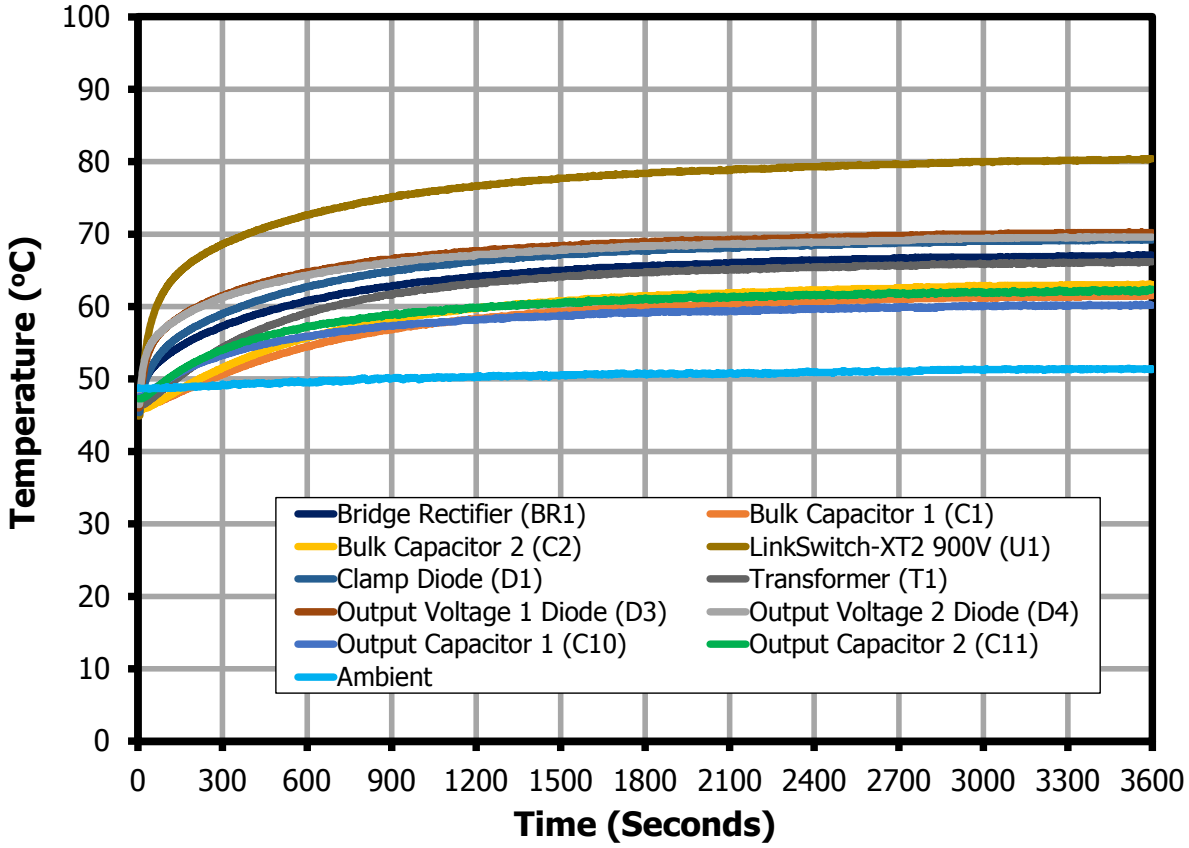


Figure 93 – Component Temperatures at 50 ºC Ambient.

Component	Final Temperature (ºC)
Bridge Rectifier (BR1)	67.0
Bulk Capacitor 1 (C1)	61.5
Bulk Capacitor 2 (C2)	63.0
LinkSwitch-XT2 900 V (U1)	80.4
Clamp Diode (D1)	69.2
Transformer (T1)	66.2
Output Voltage 1 Diode (D3)	70.2
Output Voltage 2 Diode (D4)	69.6
Output Capacitor 1 (C10)	60.2
Output Capacitor 2 (C11)	62.4
Ambient	51.4

11.3.2 *350 VAC, 50 ºC*

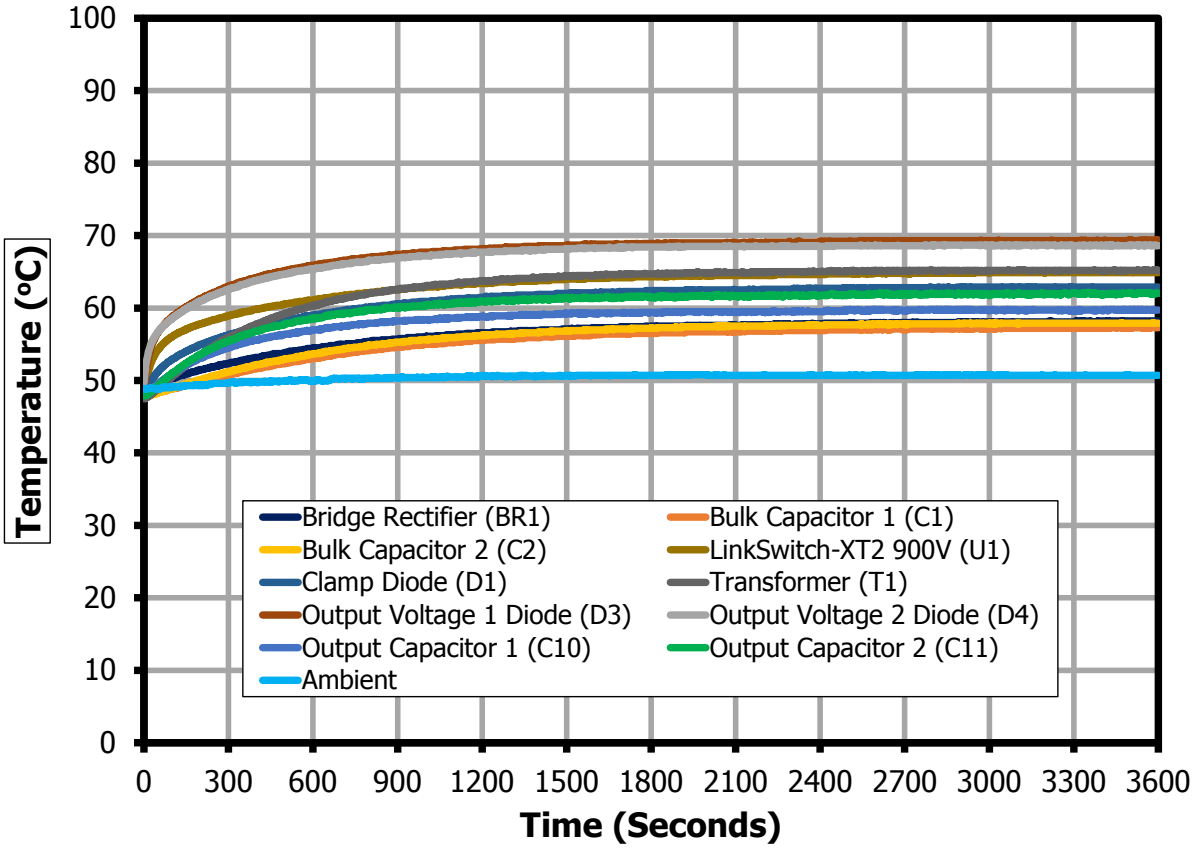


Figure 94 – Component Temperatures at 50 ºC Ambient.

Component	Final Temperature (ºC)
Bridge Rectifier (BR1)	58.2
Bulk Capacitor 1 (C1)	57.3
Bulk Capacitor 2 (C2)	57.9
LinkSwitch-XT2 900 V (U1)	64.9
Clamp Diode (D1)	62.9
Transformer (T1)	65.2
Output Voltage 1 Diode (D3)	69.4
Output Voltage 2 Diode (D4)	68.6
Output Capacitor 1 (C10)	59.7
Output Capacitor 2 (C11)	62
Ambient	50.7

12 Conducted EMI

12.1 EMI Equipment and Load

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Yokogawa W310E digital power meter.
4. Chroma measurement test fixture, model A662003.
5. Resistor load with input voltage set at 115 VAC.

12.2 Test Set-up

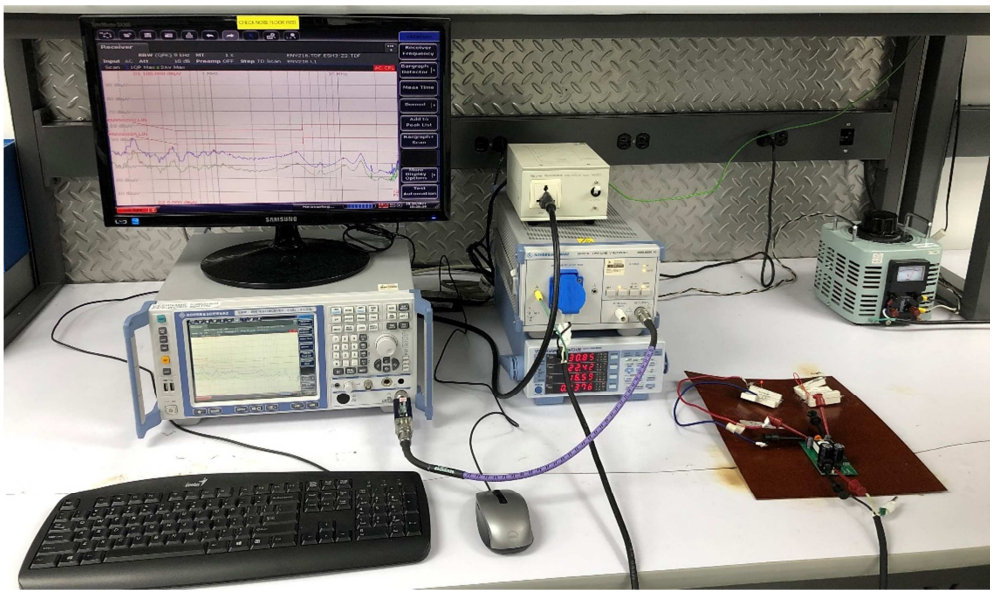


Figure 95 – Conducted EMI Test Set-up.

12.3 **EMI Test Results**

12.3.1 *115 VAC, Floating Output*

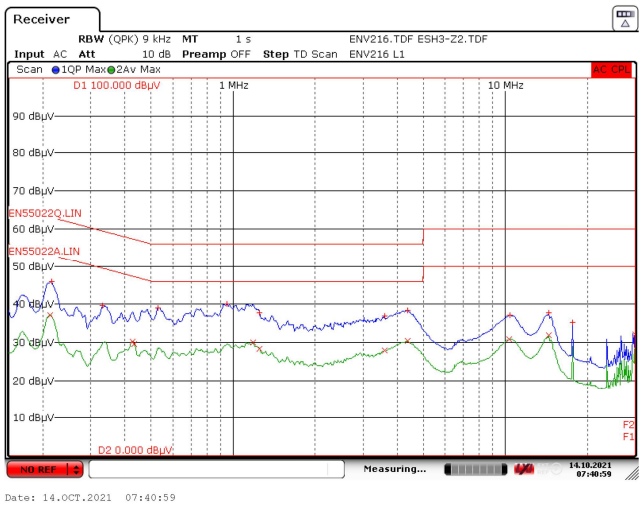


Figure 96 – Line.
Upper: Lowest Peak Delta Limit:
-15.98 dB, 946.6 kHz.
Lower: Lowest Average Delta Limit:
-15.68 dB, 4.3801 MHz.

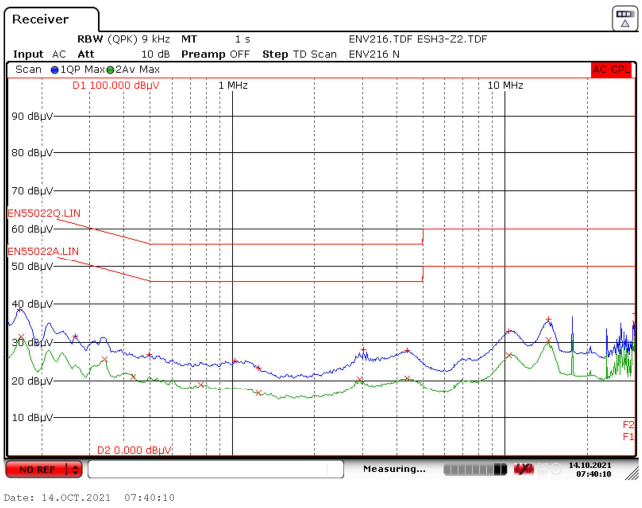


Figure 97 – Neutral.
Upper: Lowest Peak Delta Limit:
-22.45 dB, 29.9311 MHz.
Lower: Lowest Average Delta Limit:
-14.98 dB, 29.9311 MHz.

12.3.2 *230 VAC, Floating Output*

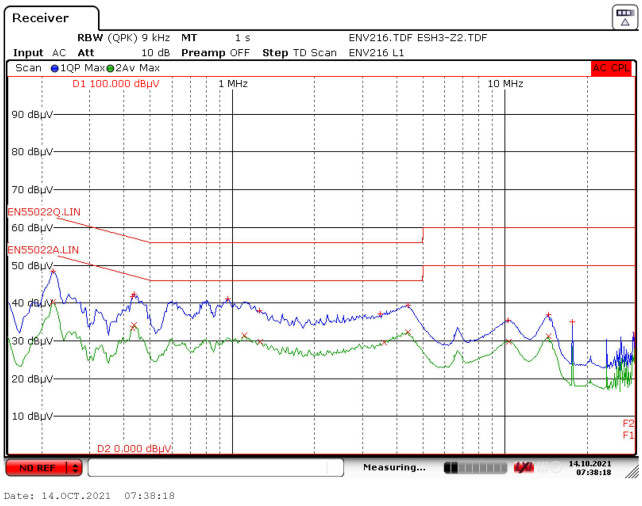


Figure 98 – Line.
Upper: Lowest Peak Delta Limit:
-14.3 dB, 219.85 kHz.
Lower: Lowest Average Delta Limit:
-12.59 dB, 219.85 kHz.

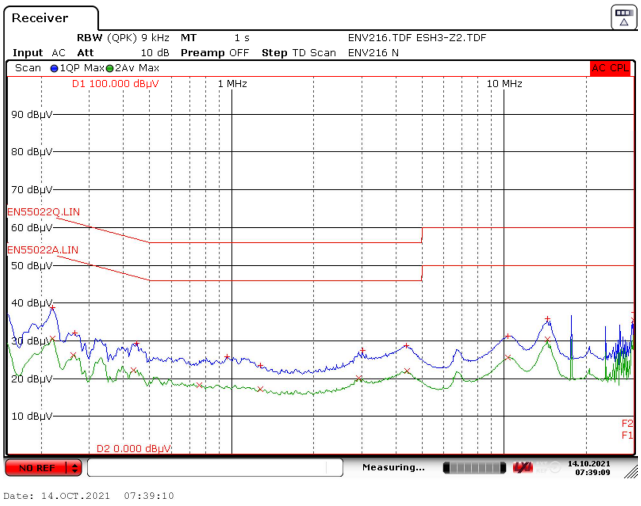


Figure 99 – Neutral.
Upper: Lowest Peak Delta Limit:
-22.38 dB, 29.9311 MHz.
Lower: Lowest Average Delta Limit:
-14.51 dB, 29.9311 MHz.

13 Line Surge

The unit was subject to ±6000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

13.1 Differential Surge Test

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number of Strikes	Result
+6	0	L1 / L2	2	10	PASS
-6	0	L1 / L2	2	10	PASS
+6	90	L1 / L2	2	10	PASS
-6	90	L1 / L2	2	10	PASS
+6	180	L1 / L2	2	10	PASS
-6	180	L1 / L2	2	10	PASS
+6	270	L1 / L2	2	10	PASS
-6	270	L1 / L2	2	10	PASS

Note: In all PASS results, no damage and no auto-restart was observed.

14 Performance with External Magnetizing Interference

14.1 Test Set-up

A Neodymium Iron Boron (NdFeB) square magnet with N35 Grade, dimensions of 6.35 mm x 6.35 mm, and Gauss strength (surface Gauss) of 3451 G was placed on the transformer core such that the typical primary inductance was reduced by at least 50%.

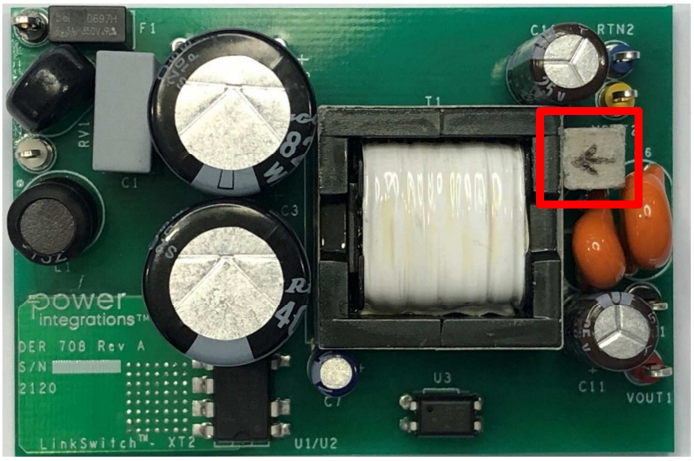


Figure 100 – Performance with External Magnetizing Interference Test Set-up.

14.2 No-Load Input Power with External Magnetizing Interference

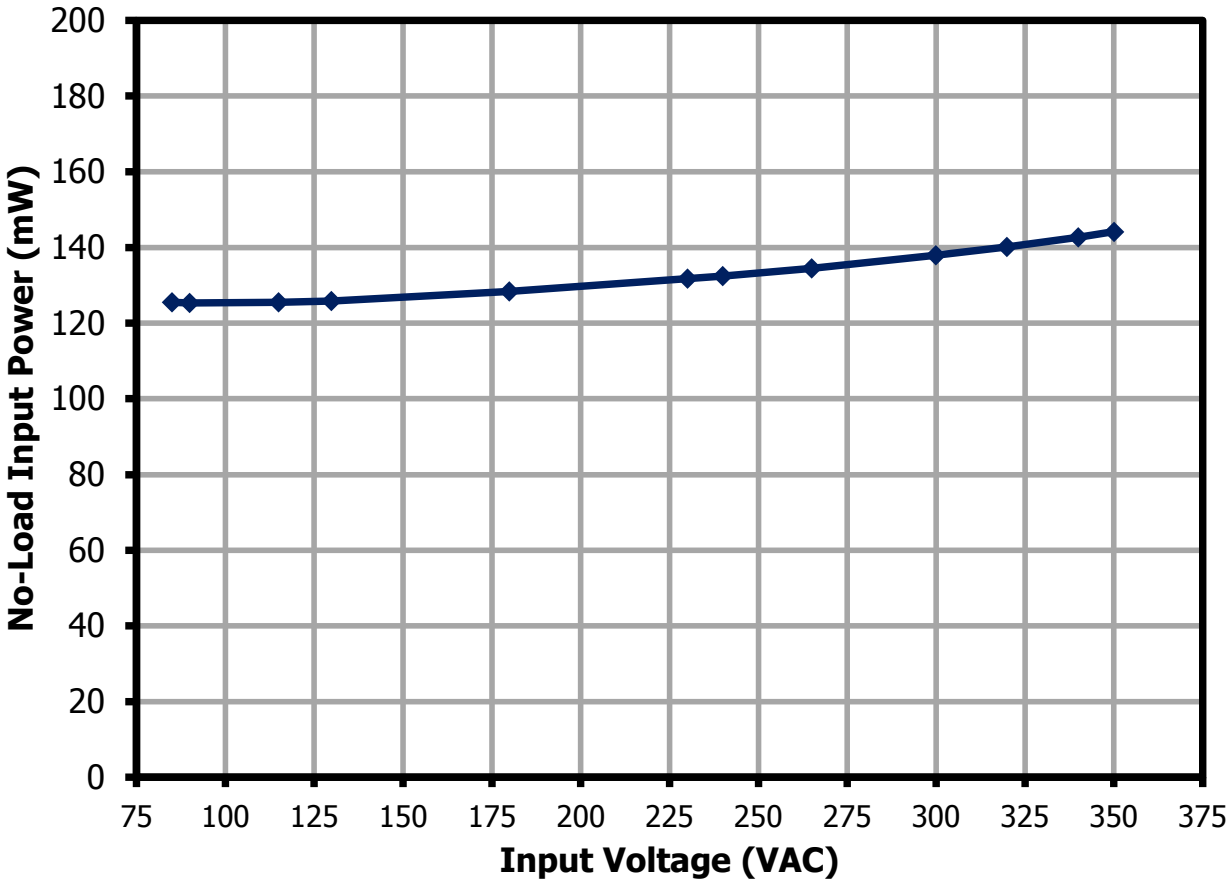


Figure 101 – No-Load Power vs. Input Line Voltage.

14.3 **Efficiency with External Magnetizing Interference**

14.3.1 *Efficiency vs Line with External Magnetizing Interference*

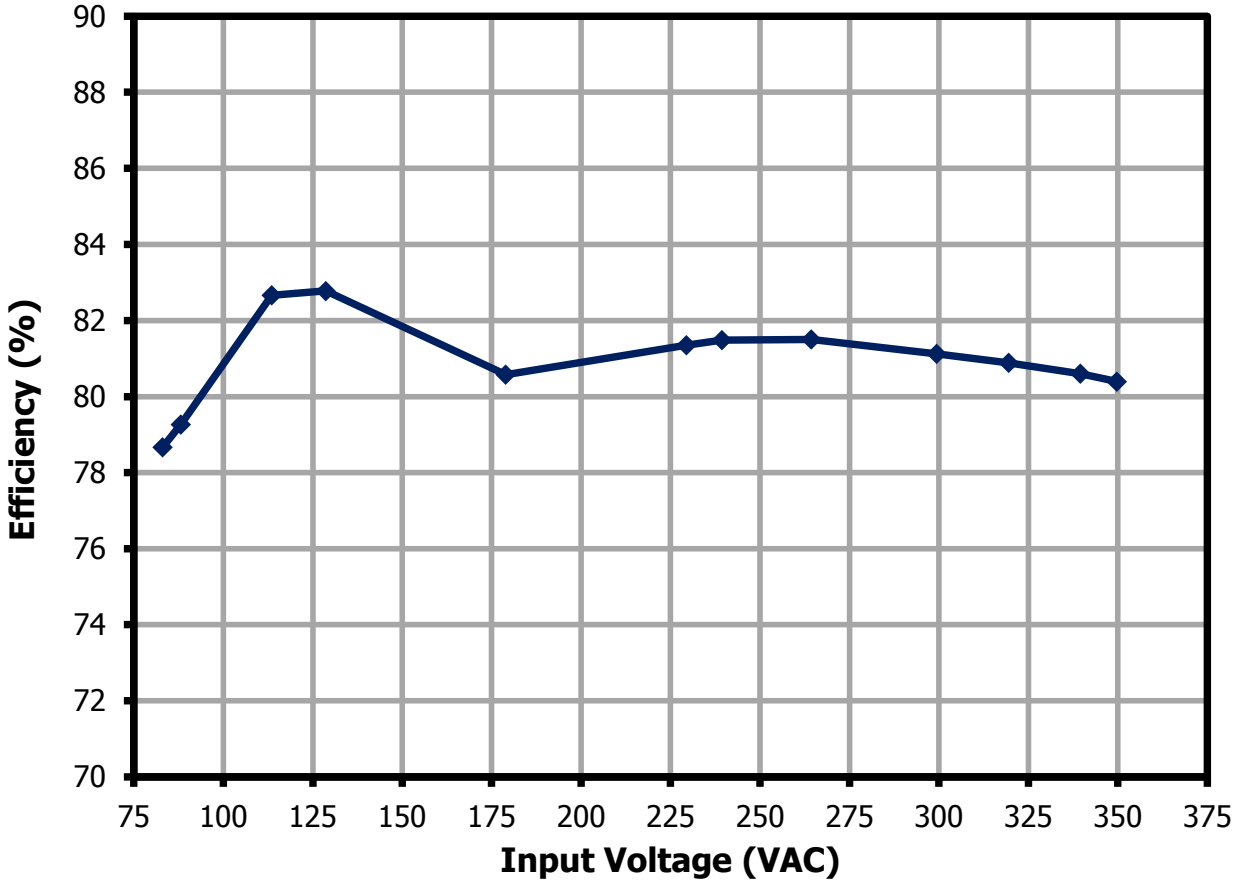


Figure 102 – Full Load Efficiency vs. Input Line Voltage.

14.3.2 *Efficiency vs Load with External Magnetizing Interference*

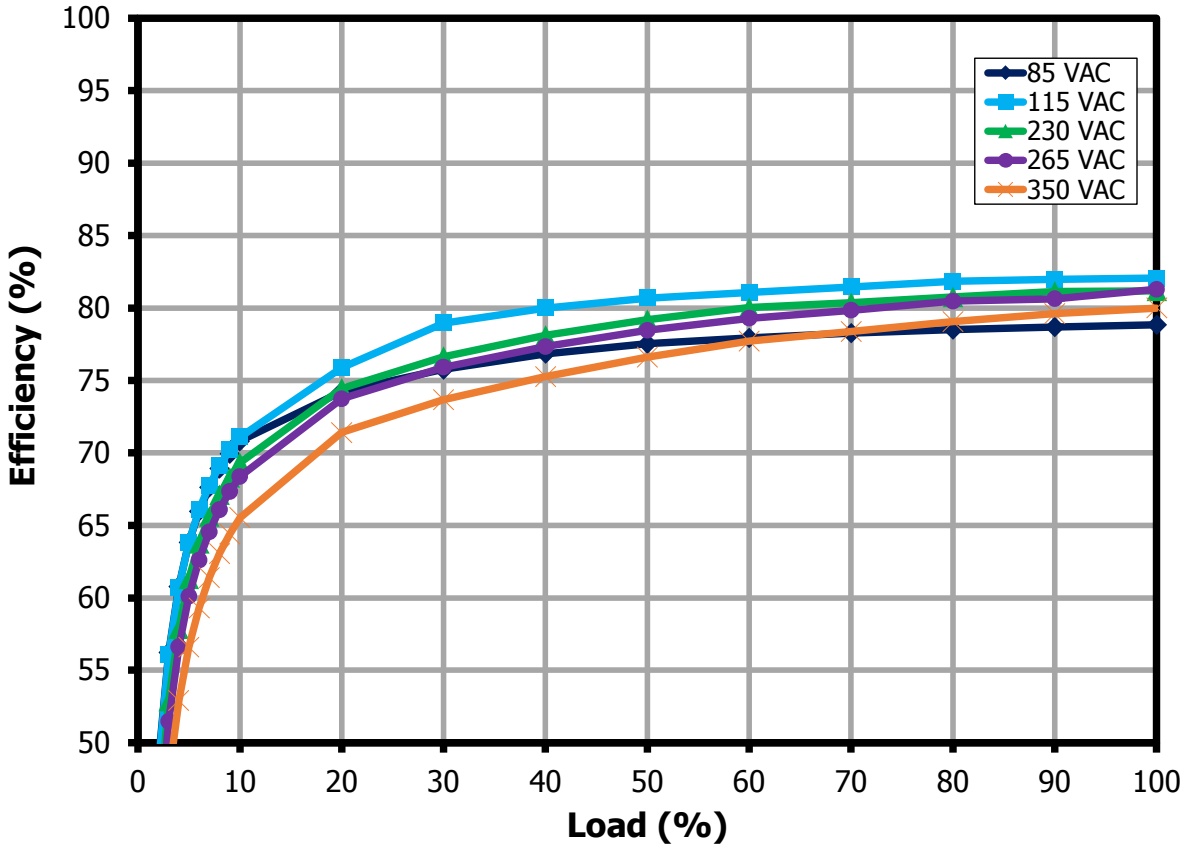


Figure 103 – Efficiency vs. Percent Load, at Different Input Line Voltages.

14.4 Output Voltage Regulation with External Magnetizing Interference

14.4.1 *18 V_{OUT1} Load Regulation with Balanced Load with External Magnetizing Interference*

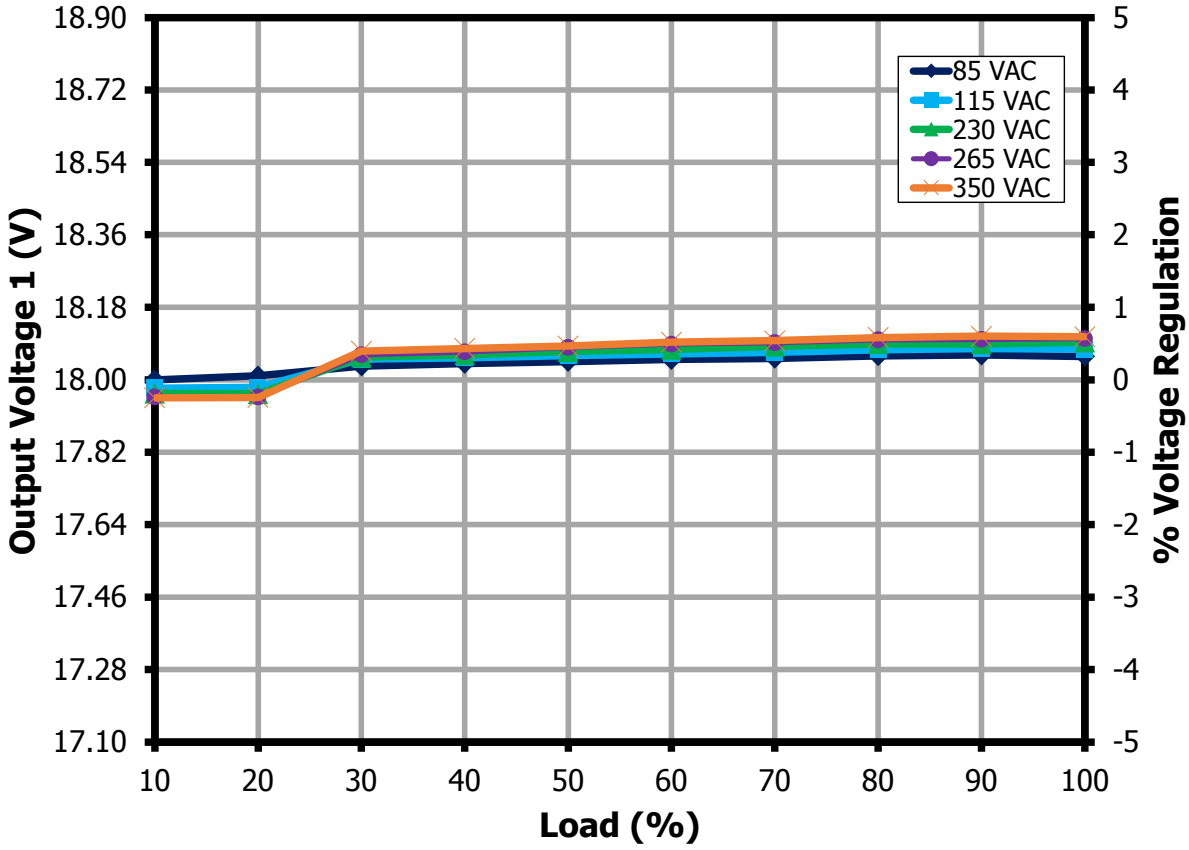


Figure 104 – 18 V_{OUT1} Load Regulation.
Condition: Simultaneous Load Decrement.

14.4.2 *18 V_{OUT2} Load Regulation with Balanced Load with External Magnetizing Interference*

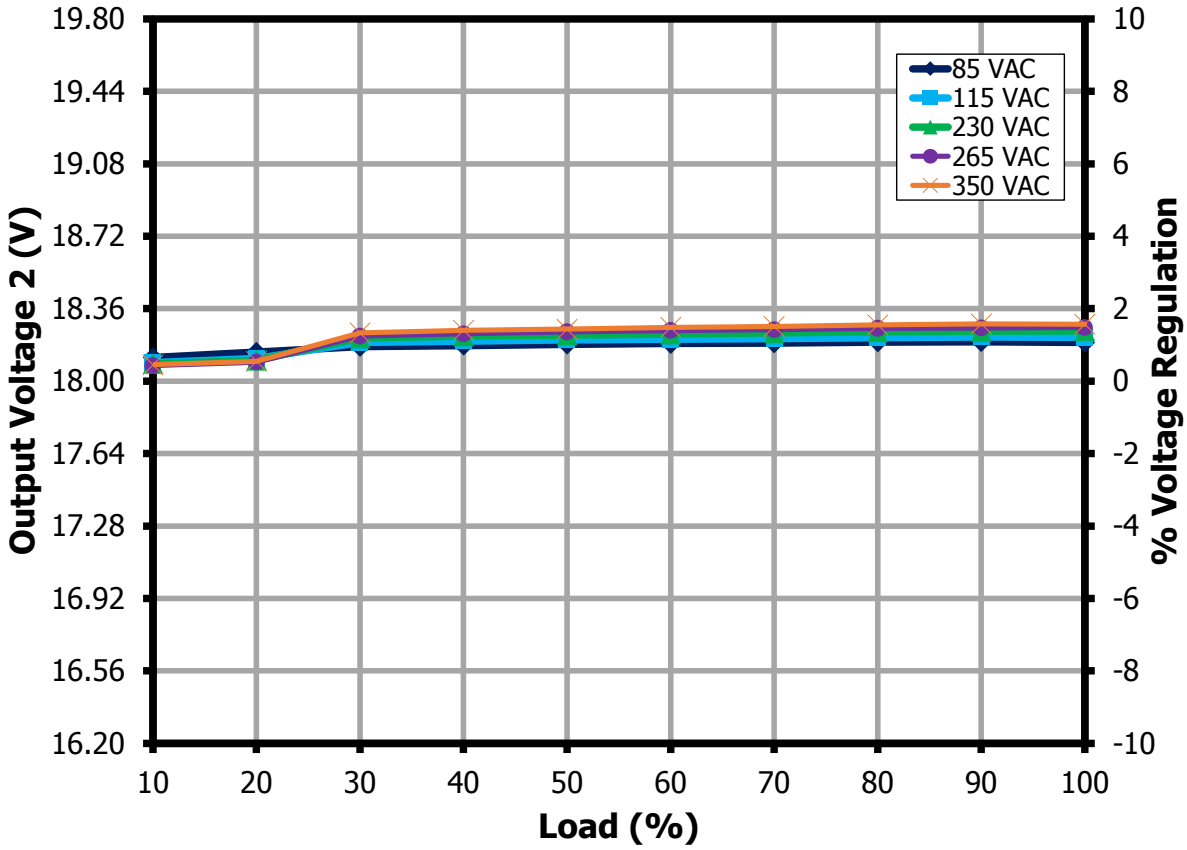


Figure 105 – 18 V_{OUT2} Load Regulation.
Condition: Simultaneous Load Decrement.

14.4.3 *Line Regulation with External Magnetizing Interference*

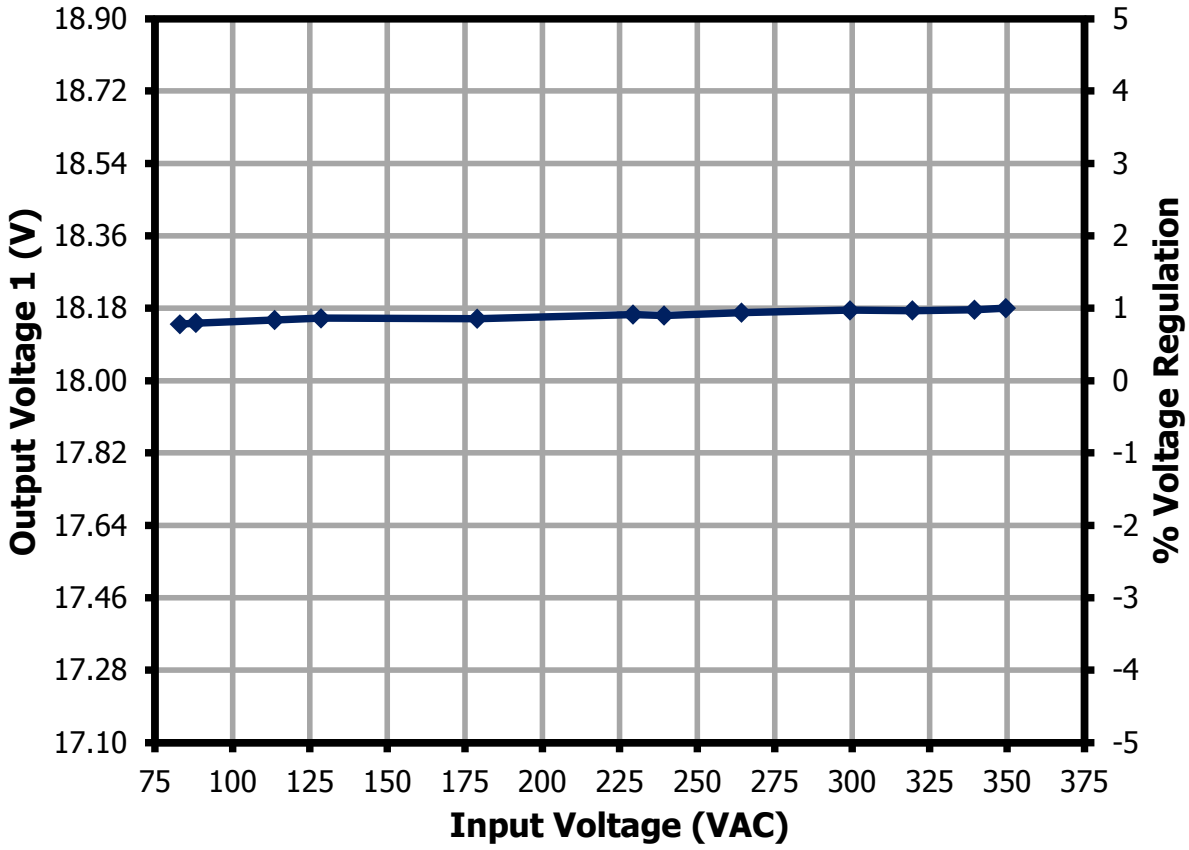


Figure 106 – 18 V_{OUT1} Output Regulation vs. Input Line Voltage.

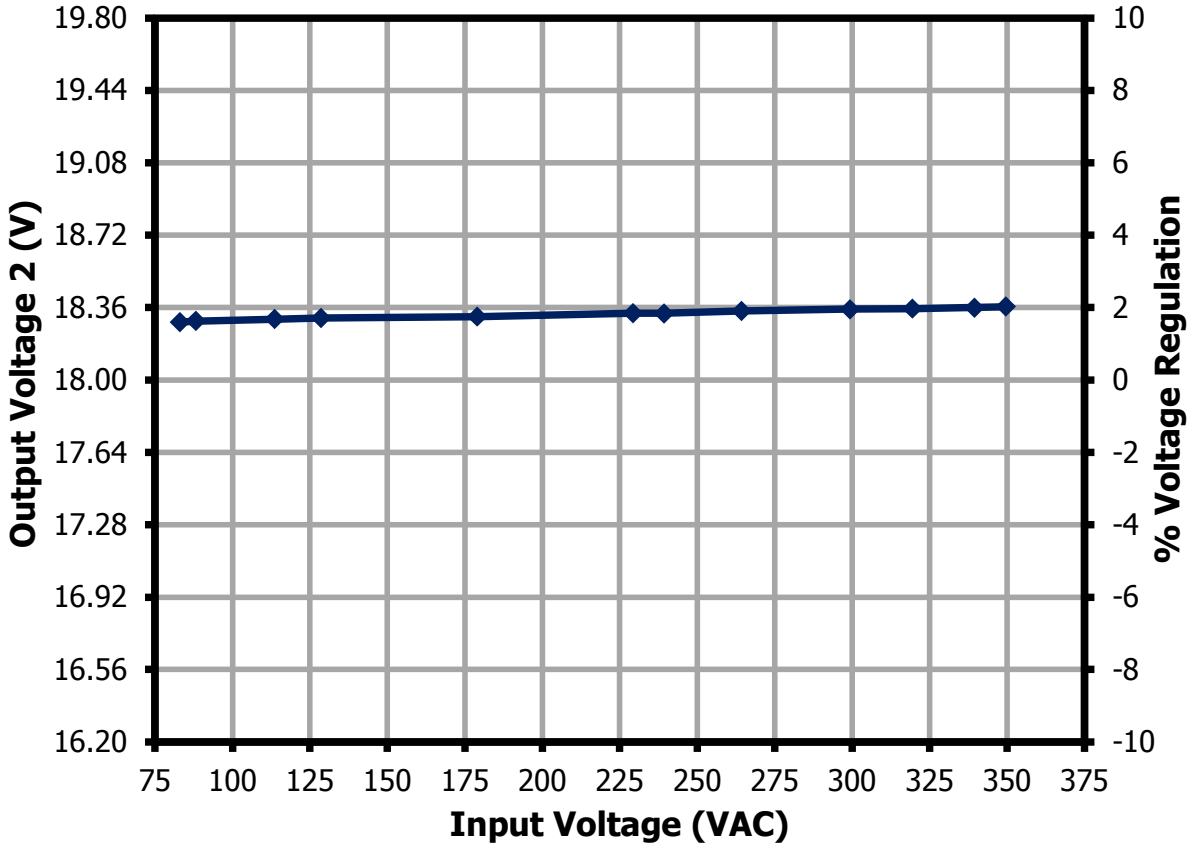


Figure 107 – 18 V_{OUT2} Output Regulation vs. Input Line Voltage.

14.5 **Drain Current and Voltage with External Magnetizing Interference**

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

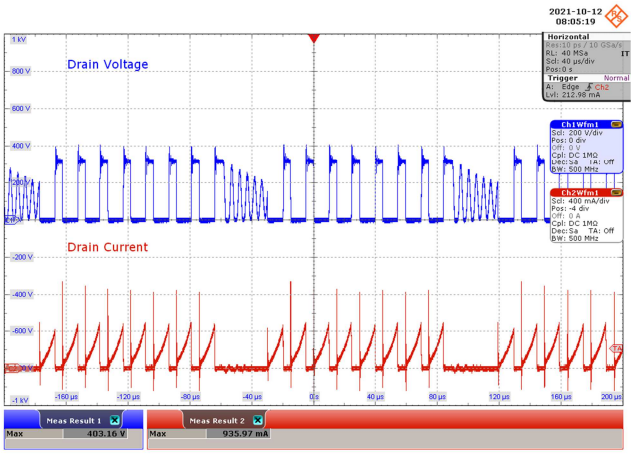


Figure 108 – 85 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 403.16 V.
$I_{DS(MAX)}$: 0.93597 A.

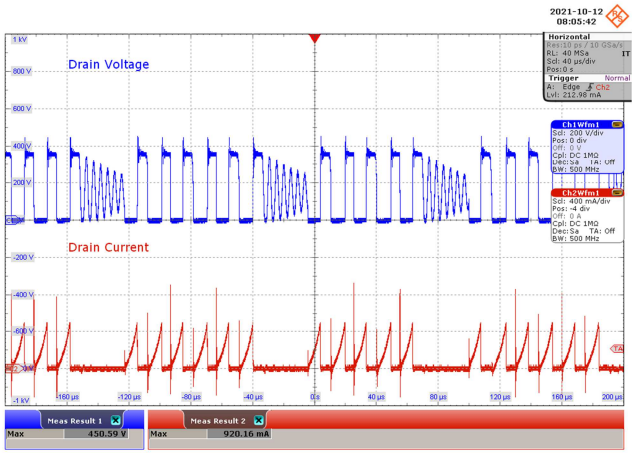


Figure 109 – 115 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 450.59 V.
$I_{DS(MAX)}$: 0.92016 A.

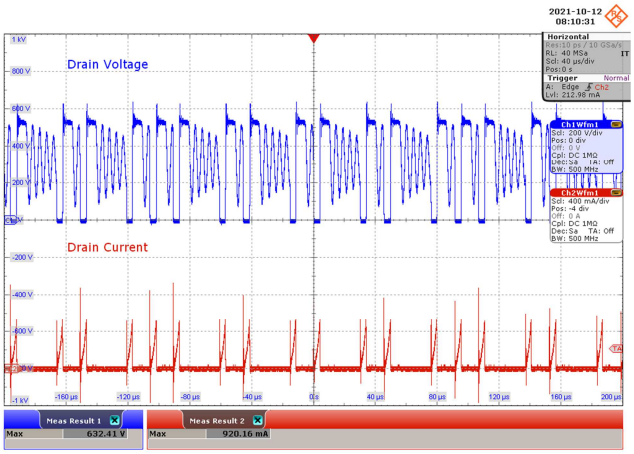


Figure 110 – 230 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 632.41 V.
$I_{DS(MAX)}$: 0.92016 A.

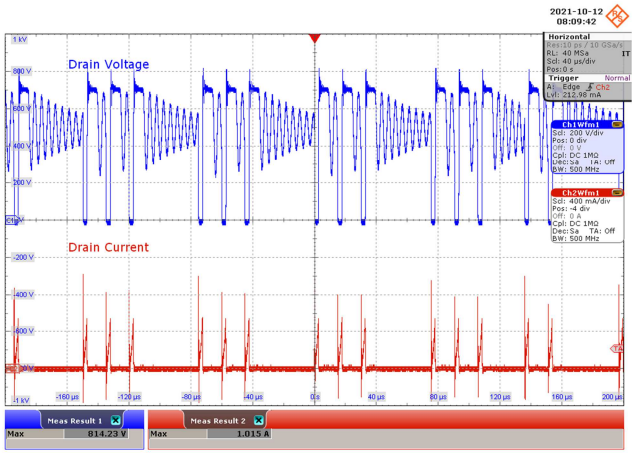


Figure 111 – 350 VAC Input.
CH1: Drain Voltage, 200 V / div., 40 µs / div.
CH2: Drain Current, 400 mA / div., 40 µs / div.
$V_{DS(MAX)}$: 814.23 V.
$I_{DS(MAX)}$: 1.0015 A.

14.6 Start-up Performance with External Magnetizing Interference

14.6.1 *18 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CC Load*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

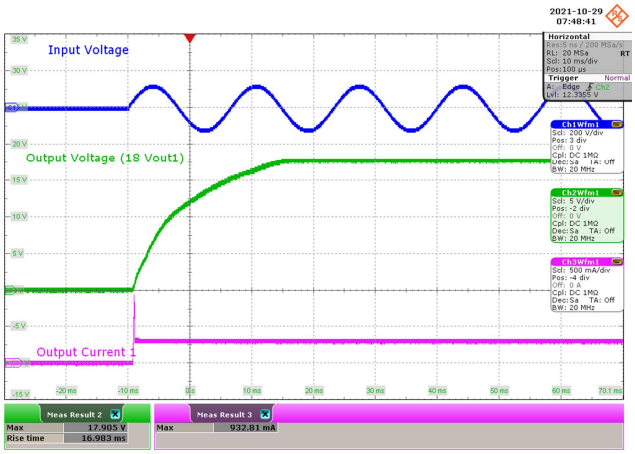


Figure 112 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 16.983 ms.

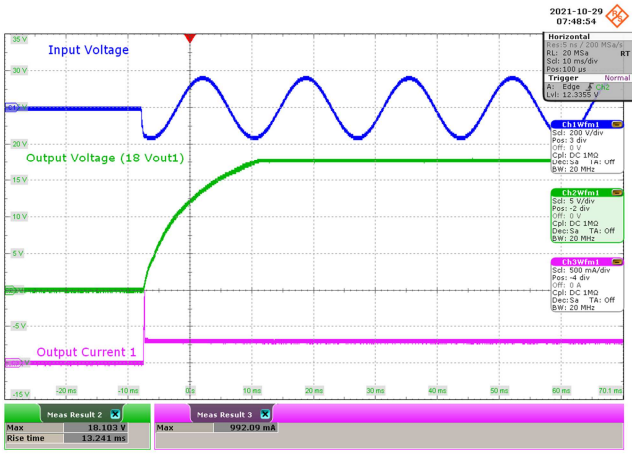


Figure 113 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 13.241 ms.

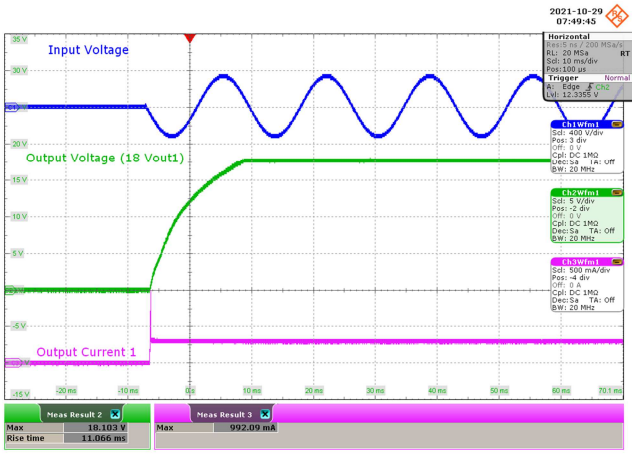


Figure 114 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 11.066 ms.

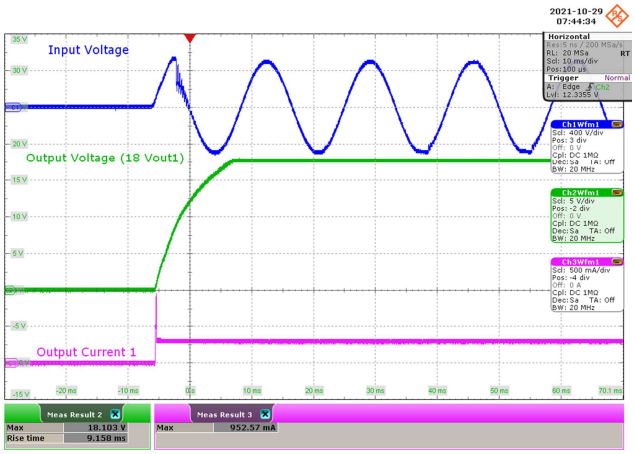


Figure 115 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 9.158 ms.

14.6.2 *18 V_{OUT1} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CR Load*

Test conditions: 18 V_{OUT1} load set to CR at 60 Ω, 18 V_{OUT2} load set to CR at 72 Ω

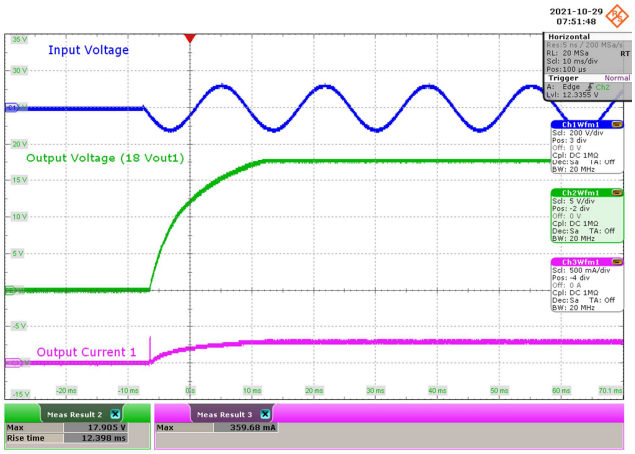


Figure 116 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 12.398 ms.

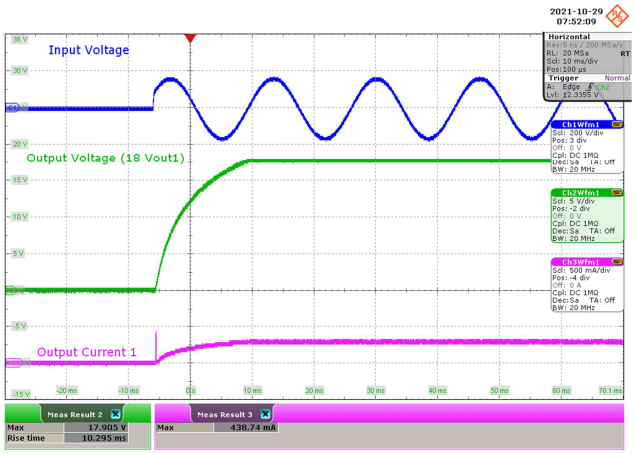


Figure 117 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 10.295 ms.

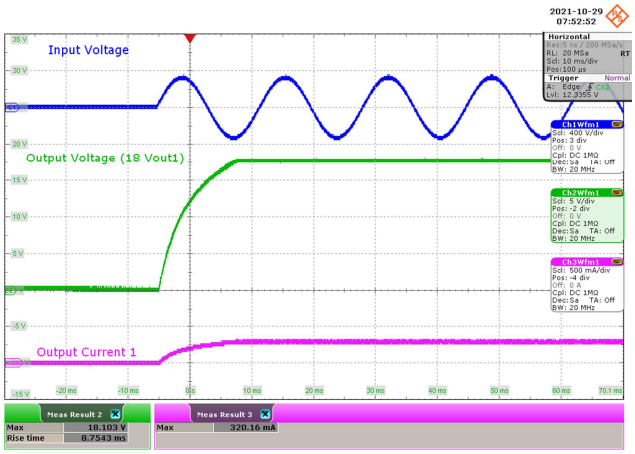


Figure 118 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 8.7543 ms.

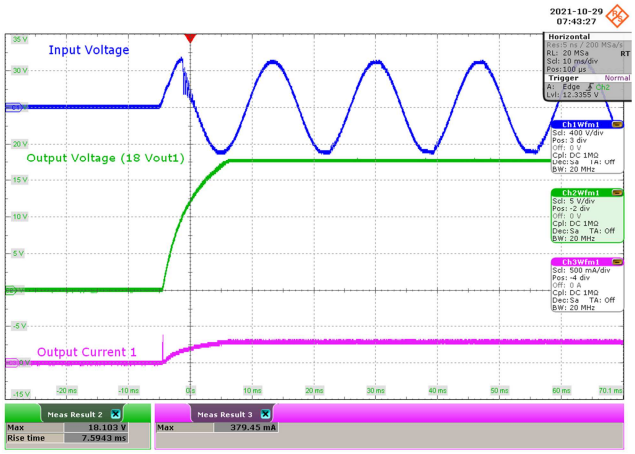


Figure 119 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 1, 5 V / div., 10 ms / div.
CH3: Output Current 1, 500 mA / div., 10 ms / div.
Rise Time: 7.5943 ms.

14.6.3 *18 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CC Load*

Test conditions: 18 V_{OUT1} load set to CR at 60 Ω, 18 V_{OUT2} load set to CR at 72 Ω

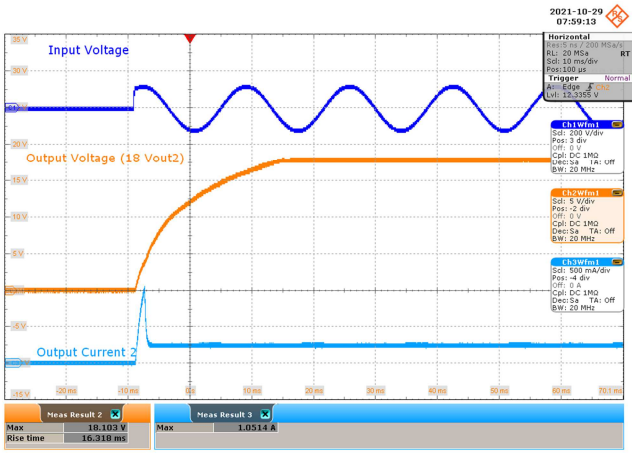


Figure 120 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 16.318 ms.

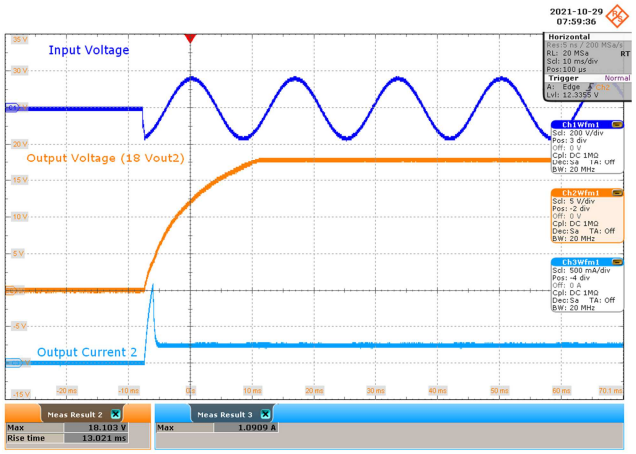


Figure 121 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 13.021 ms.

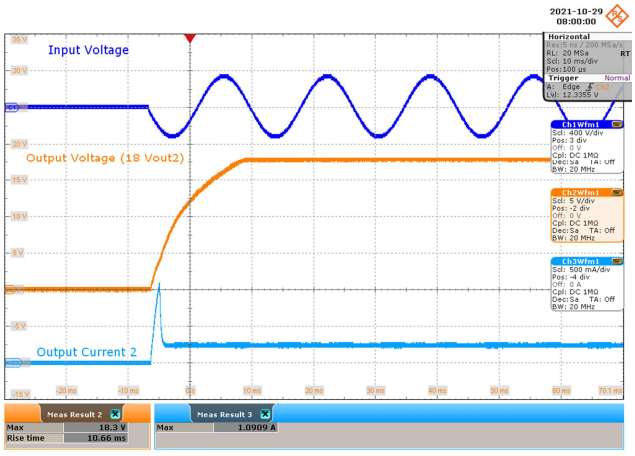


Figure 122 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 10.66 ms.

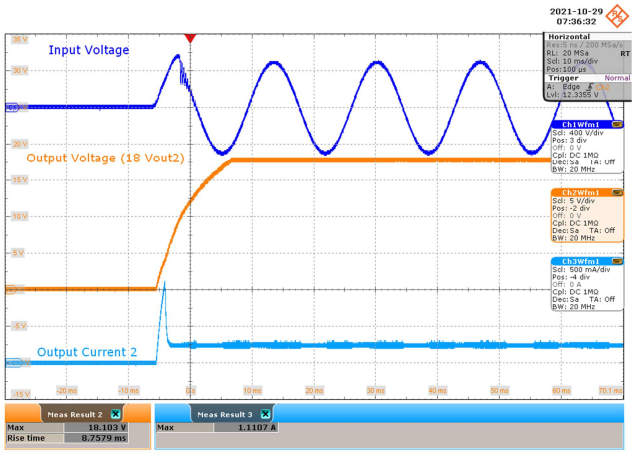


Figure 123 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CC.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 8.7579 ms.

14.6.4 *18 V_{OUT2} Start-up Operation V_{IN}, V_{OUT} and I_{OUT} with CR Load*

Test conditions: 18 V_{OUT1} load set to CR at 60 Ω, 18 V_{OUT2} load set to CR at 72 Ω

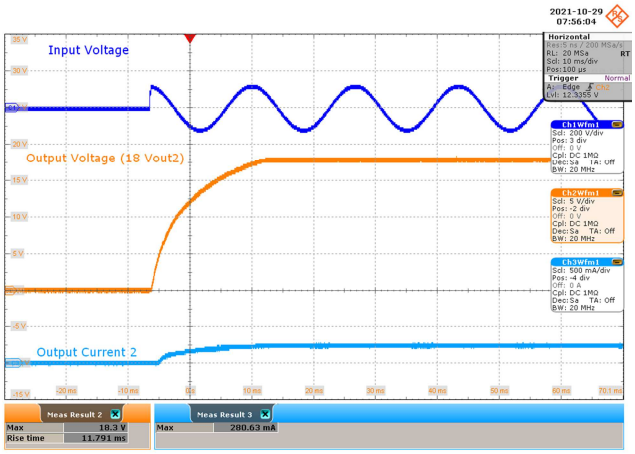


Figure 124 – 85 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 11.791 ms.

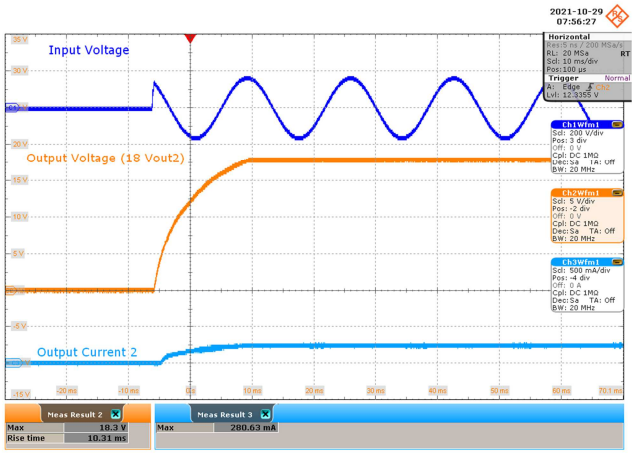


Figure 125 – 115 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 200 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 10.31 ms.

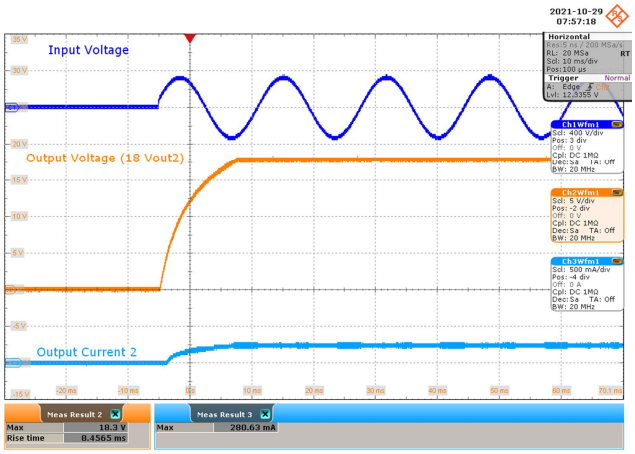


Figure 126 – 230 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 8.4565 ms.

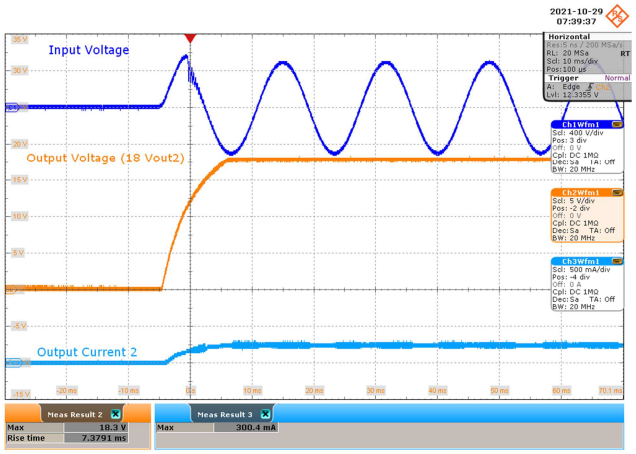


Figure 127 – 350 VAC Input. I_{OUT1} & I_{OUT2} = 100% CR.
CH1: Input Voltage, 400 V / div., 10 ms / div.
CH2: Output Voltage 2, 5 V / div., 10 ms / div.
CH3: Output Current 2, 500 mA / div., 10 ms / div.
Rise Time: 7.3791 ms.

14.6.5 *Drain Current and Drain Voltage Start-up Operation with External Magnetizing Interference*

Test conditions: 18 V_{OUT1} load set to CC at 300 mA, 18 V_{OUT2} load set to CC at 250 mA

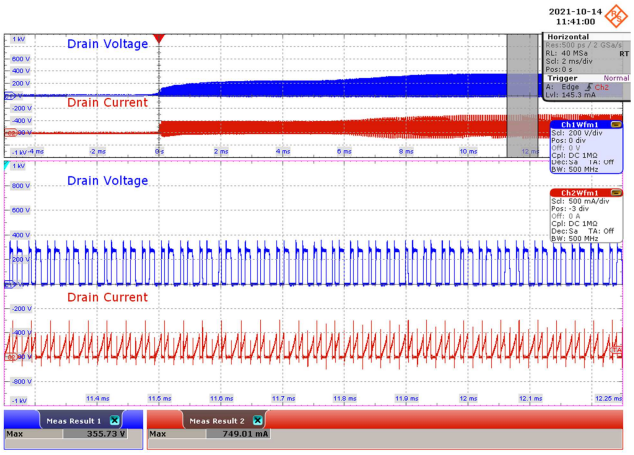


Figure 128 – 85 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 355.73 V.
$I_{DS(MAX)}$: 0.74901 A.

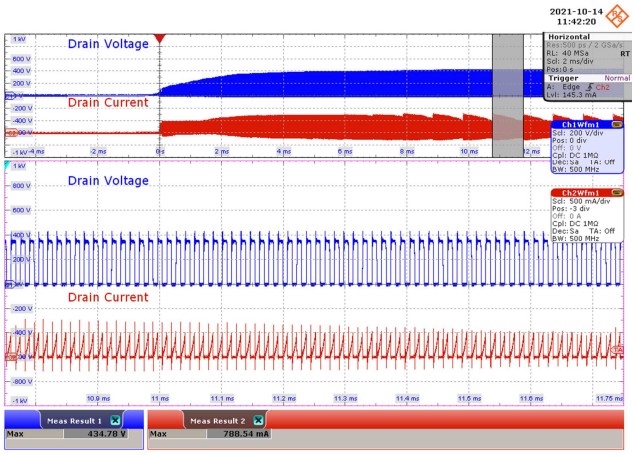


Figure 129 – 115 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 434.78 V.
$I_{DS(MAX)}$: 0.78854 A.

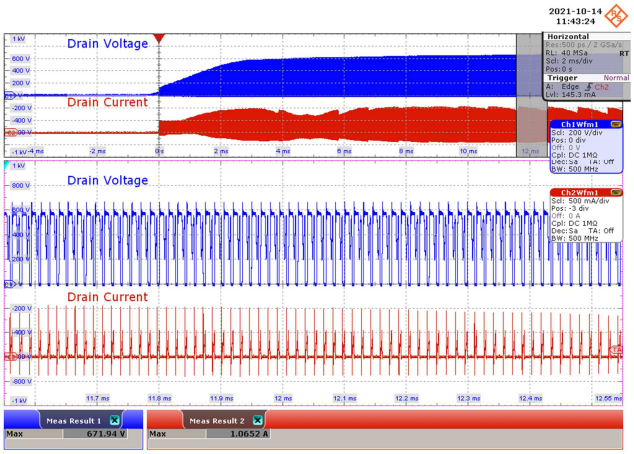


Figure 130 – 230 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 671.94 V.
$I_{DS(MAX)}$: 1.0652 A.

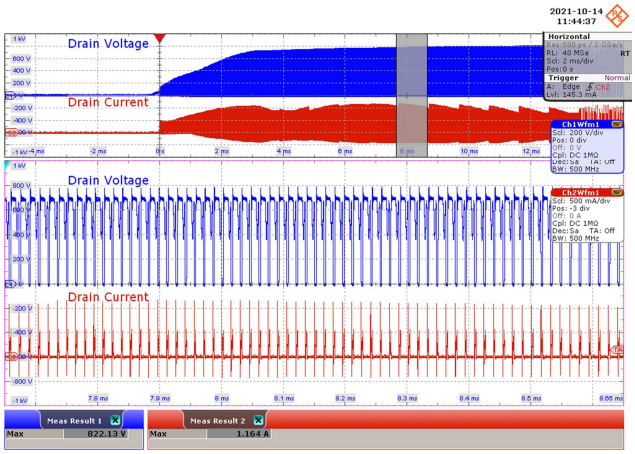


Figure 131 – 350 VAC Input.
CH1: Drain Voltage, 200 V / div., 2 ms / div.
CH2: Drain Current, 500 mA / div., 2 ms / div.
Zoom: 100 µs / div.
$V_{DS(MAX)}$: 822.13 V.
$I_{DS(MAX)}$: 1.164 A.

14.7 Thermal Performance with External Magnetizing Interference at Room Temperature

14.7.1 *85 VAC, Room Temperature*

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	18 V_{OUT1} Output Diode (D3)	18 V_{OUT2} Output Diode (D4)	Ambient Temperature
65.3 ºC	55.8 ºC	47.1 ºC	56.7 ºC	55.2 ºC	53.3 ºC	24.4 ºC

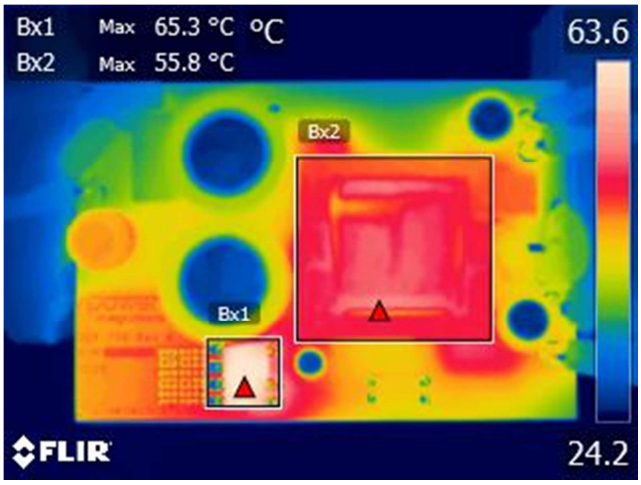


Figure 132 – Ambient = 24.2 ºC.
Bx1, U1: 65.3 ºC.
Bx2, T1: 55.8 ºC.

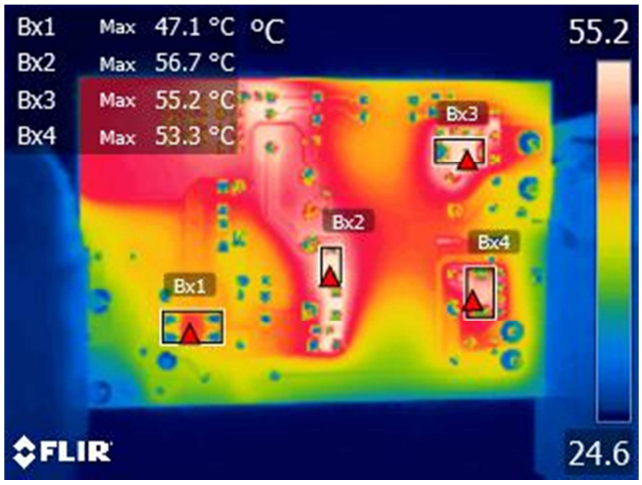


Figure 133 – Ambient = 24.6 ºC.
Bx1, BR1: 47.1 ºC.
Bx2, D1: 56.7 ºC.
Bx3, D3: 55.2 ºC.
Bx4, D4: 53.3 ºC.

14.7.2 *350 VAC, Room Temperature*

LinkSwitch-XT2 900 V (U1)	Transformer (T1)	Bridge Rectifier (BR1)	Clamp Diode (D1)	18 V_{OUT1} Output Diode (D3)	18 V_{OUT2} Output Diode (D4)	Ambient Temperature
56.6 ºC	57.9 ºC	39.5 ºC	52.6 ºC	58.1 ºC	55.6 ºC	24.7 ºC

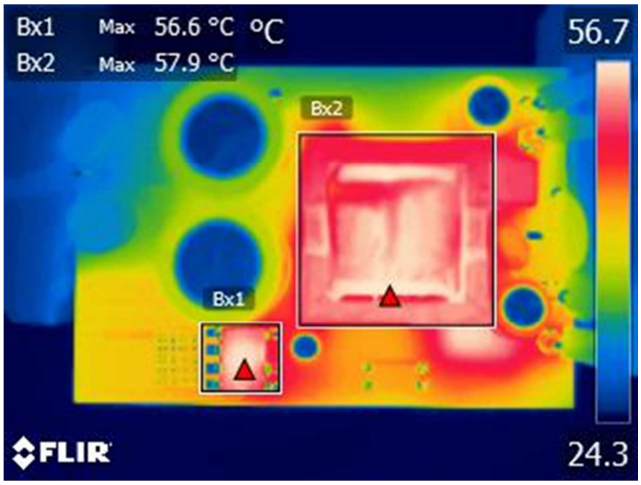


Figure 134 – Ambient = 24.3 ºC.
Bx1, U1: 56.6 ºC.
Bx2, T1: 57.9 ºC.

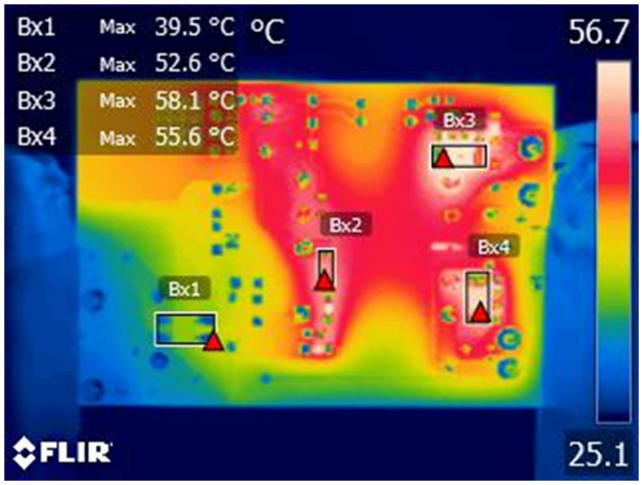


Figure 135 – Ambient = 25.1 ºC.
Bx1, BR1: 39.5 ºC.
Bx2, D1: 52.6 ºC.
Bx3, D3: 58.1 ºC.
Bx4, D4: 55.6 ºC.

14.8 **EMI with External Magnetizing Interference Test Results**

14.8.1 *115 VAC, Floating Output*

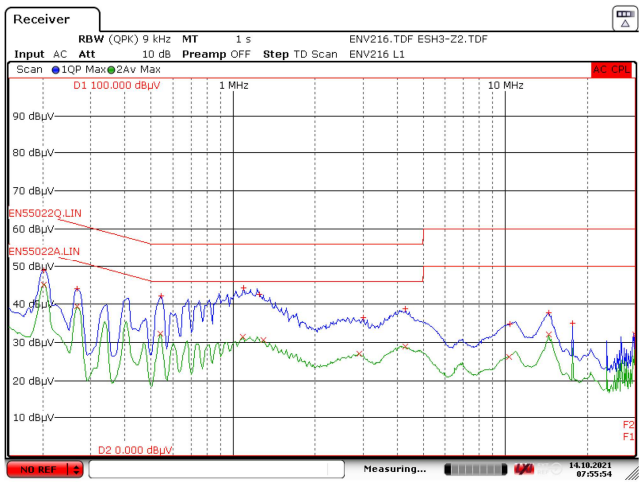


Figure 136 – Line.
Upper: Lowest Peak Delta Limit:
-11.73 dB, 1.0906 MHz.
Lower: Lowest Average Delta Limit:
-8.44 dB, 201.85 kHz.

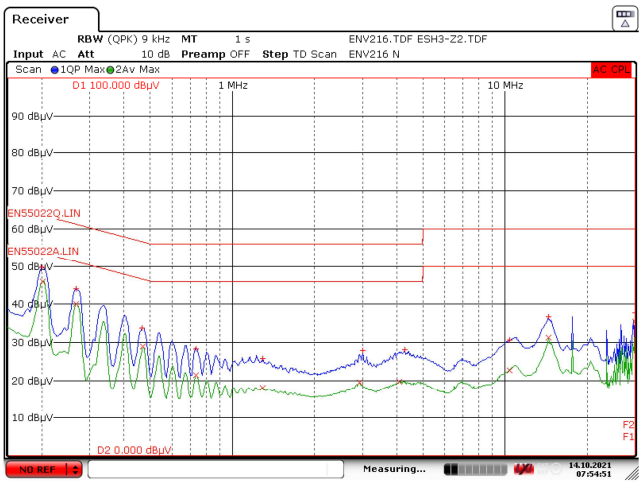


Figure 137 – Neutral.
Upper: Lowest Peak Delta Limit:
-13.95 dB, 199.6 kHz.
Lower: Lowest Average Delta Limit:
-7.52 dB, 201.85 kHz.

14.8.2 *230 VAC, Floating Output*

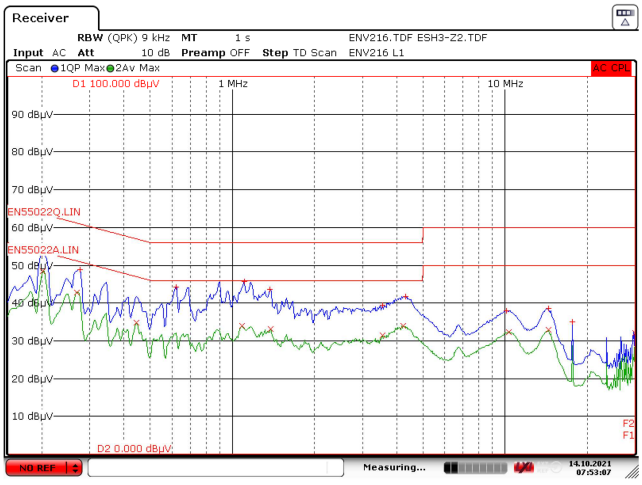


Figure 138 – Line.
Upper: Lowest Peak Delta Limit:
-10.39 dB, 1.1086 MHz.
Lower: Lowest Average Delta Limit:
-5.05 dB, 201.85 kHz.

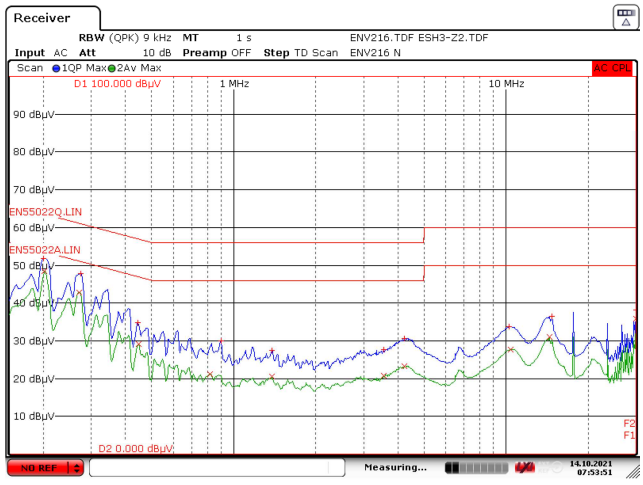


Figure 139 – Neutral.
Upper: Lowest Peak Delta Limit:
-11.86 dB, 199.6 kHz.
Lower: Lowest Average Delta Limit:
-5.16 dB, 201.85 kHz.

15 Revision History

Date	Author	Revision	Description & Changes	Reviewed
20-Dec-21	MT/CD	1.0	Initial Release.	Mktg & Apps

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