Design Example Report

Title	***2.5 W Non-Isolated Supply Using LinkSwitch™-CV LNK623D***
Specification	85 VAC – 265 VAC Input; 5 V, 0.5 A Output
Application	Home and Building Automation
Author	Applications Engineering Department
Document Number	DER-831
Date	October 8, 2019
Revision	1.0

Summary and Features

- Highly integrated solution with LNK623D
- Non-isolated 5 V/500 mA output (±7%) for WiFi and relay power
- Low component count with integrated 725 V MOSFET, current sensing and protection
- Compact solution 1” x 1” x 0.56”
- <150 mW no-load input power at 230 VAC
- 0 to 40˚C ambient temperature operation range
- Optimized for <20 dB audible noise performance
- 1 KV differential line surge protection
- Load short-circuit protection
- Over-temperature protection with hysteretic recovery
- EN55022B conducted EMI compliant

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Important Note:
Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

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1 Introduction

This document is an engineering report describing a non-isolated 5 V, 0.5 A supply utilizing a device from the LinkSwitch-CV family of ICs, specifically using LNK623D.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.

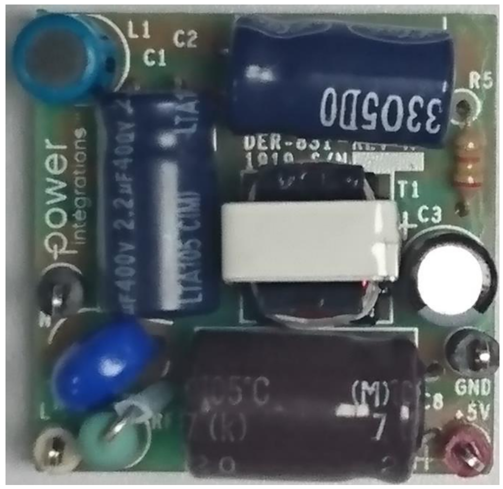

Figure 1 – Populated Circuit Board Photograph, Top.

Figure 2 – Populated Circuit Board Photograph, Bottom.

2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
Input						
Voltage	V_{IN}	85		265	VAC	2 Wire – no P.E.
Frequency	f_{LINE}	47	50/60	63	Hz	
No-load Input Power				160	mW	265VAC Input.
Output						
Output Voltage	V_{OUT}		5.00		V	±7% PCB Connector Side.
Output Ripple Voltage	V_{RIPPLE}			300	mVpp	Measured at the PCB Connector.
Output Current	I_{OUT}	0.05		0.5	A	
Continuous Output Power	P_{OUT}			2.5	W	
Efficiency						
Average 25%, 50%, 75%, and 100%	$\eta_{AVE[BRD]}$	64			%	DoE Level VI, Basic Voltage.
Environmental						
Conducted EMI		CISPR22B / EN55022B Load floating				Resistive Load, 6 dB Margin.
Differential Line Surge		1			kV	1.2/50 µs surge, IEC 61000-4-5, Series Impedance: Differential Mode: 2 Ω.
Ambient Temperature	T_{AMB}	0		40	ºC	Free Convection, Sea Level in Sealed Enclosure.

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3 Schematic Diagram

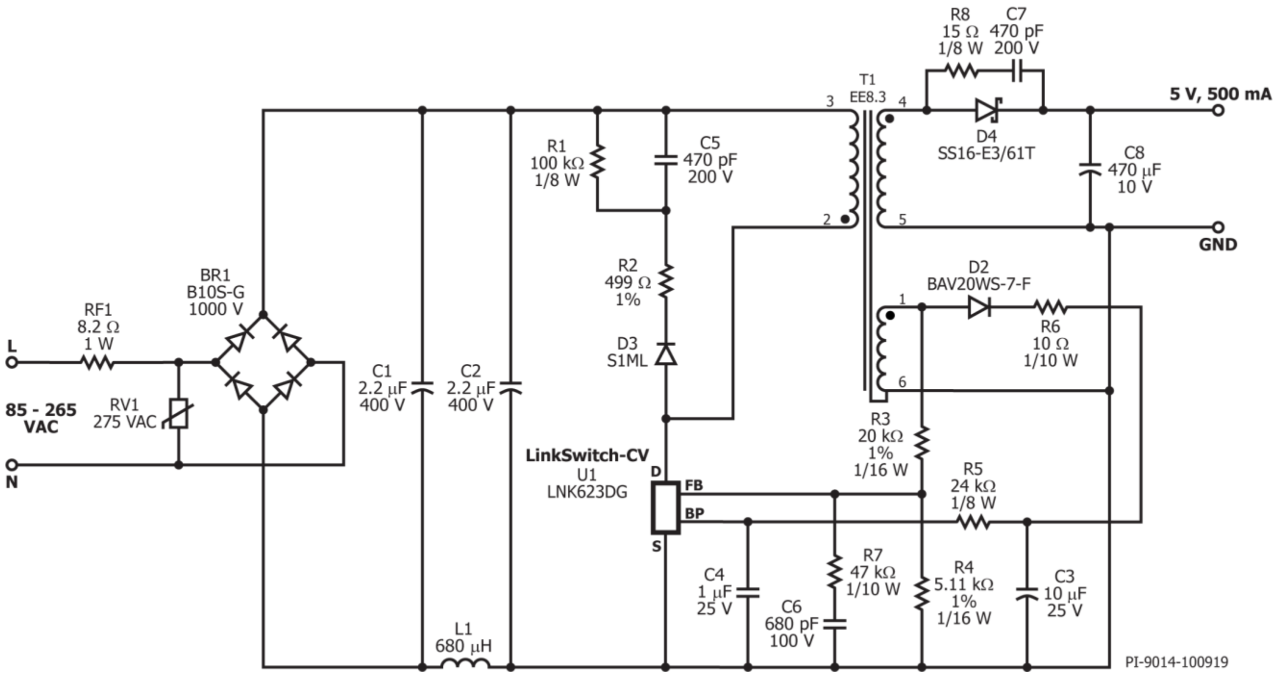

Figure 3 – Schematic.

4 Circuit Description

4.1 *Input EMI Filtering*

Resistor RF1 is fusible, flameproof, wire-wound type and functions as a fuse and inrush current limiter which provide protection against catastrophic failure of components of the primary-side and limits the inrush current when the power supply is connected to the AC input supply due to low impedance of the input capacitors, C1 and C2, during start-up operation.

Varistor RV1 clamps the AC input voltage across the power supply against surge and voltage transients.

Bridge rectifier BR1 rectifies the AC line voltage and provides a full wave rectified DC across the input capacitors, C1 and C2.

Capacitors C1 and C2 provide filtering of the rectified AC Input and together with L1 forming a π (pi) filter to attenuate differential mode EMI.

4.2 *LNK623D Primary*

The LNK623D device (U1) incorporates the power switching device, oscillator, CV control engine, and start-up and protection function on a single IC. The integrated 725 V power MOSFET allows sufficient voltage margins across universal AC input applications. The device is powered from the BP pin with the decoupling capacitor C4 via the bias circuit D2, R5, R6 and C3 along with the bias/feedback winding of transformer T1. The resistor R6 helps dampen the ringing on the bias winding voltage. The resistor R5 limits the BP pin current.

The rectified and filtered input voltage is applied to one end of the transformer T1 primary winding. The other side of the T1 primary winding is driven by the internal MOSFET of U1. A low cost RCD clamp formed by D3, R1, R2 and C5 limits the peak drain voltage due to the effects of transformer leakage reactance and output trace inductance.

4.3 *Output Rectification and Filtering*

Transformer T1 secondary voltage is rectified by a Schottky barrier-type diode D4 and filtered by the low ESR output capacitor C8.

4.4 *Output Regulation*

The LNK623D regulates the output using ON/OFF control for CV regulation. The output voltage is sensed by the bias/feedback winding on transformer T1. The feedback resistors R3 and R4 were selected using standard 1% tolerance resistor values to center both the nominal output voltage. Resistor R7 and capacitor C6 across the feedback pin improve transient response and output voltage ripple measurements.

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5 PCB Layout

PCB copper thickness is 1 oz (2.8 mils / 70 μm) unless otherwise stated.

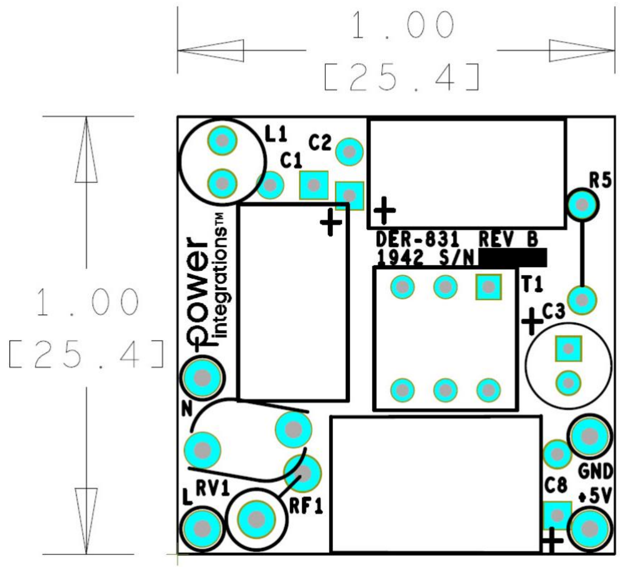

Figure 4 – Printed Circuit Layout, Top.

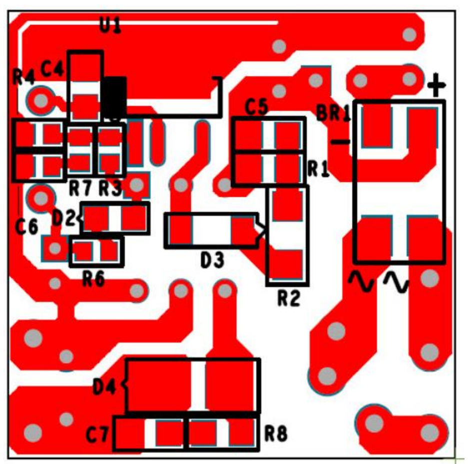

Figure 5 – Printed Circuit Layout, Bottom.

6 Bill of Materials

Item	Qty	Ref Des	Description	Mfg Part Number	Mfg
1	1	BR1	1000 V, 0.8 A, Bridge Rectifier, SMD, MBS-1, 4-SOIC	B10S-G	Comchip
2	1	C1, C2	2.2 μF, 400 V, Electrolytic, (6.3 x 11)	TAB2GM2R2E110	Ltec
3	1	C3	10 μF, 20%, 25 V, Electrolytic,-55°C ~ 105°C, 1000 Hrs @ 105°C, Gen Purpose, (5 x 6)	UMT1E100MDD1TP	Nichicon
4	1	C4	1 μF, ±10%, 25 V, Ceramic, X7R, 0805	GCM21BR71E105KA56L	Murata
5	1	C5	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
6	1	C6	680 pF 100 V, Ceramic, NP0, 0603	CGA3E2C0G2A681J	TDK
7	1	C7	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
8	1	C8	470 μF, 10 V, Electrolytic, Very Low ESR, 72 mΩ, (8 x 11.5)	EKZE100ELL471MHB5D	Nippon Chemi-Con
9	1	D2	200 V, 200 mW, Diode, SOD323	BAV20WS-7-F	ON Semi
10	1	D3	1K V, 1 A, Standard Recovery, SMA	S1ML	TAIWAN SEMI
11	1	D4	60 V, 1 A, Schottky, DO-214AC	SS16-E3/61T	Vishay
12	1	L1	680 μH, 0.25 A, 5.5 x 10.5 mm	SBC1-681-251	Tokin
13	1	R1	RES, 100 kΩ, 5%, 1/8 W, Automotive, AEC-Q200,Thick Film, 0805	ERJ-6GEYJ104V	Panasonic
14	1	R2	RES, 499 R, 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF4990V	Panasonic
15	1	R3	RES, 20 kΩ, 1%, 1/16 W, Automotive, AEC-Q200,Thick Film, 0603	ERJ-3EKF2002V	Panasonic
16	1	R4	RES, 5.11 k, 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF5111V	Panasonic
17	1	R5	RES, 24 kΩ, 5%, 1/8 W, Carbon Film	CF18JT24K0	Stackpole
18	1	R6	RES, 10 Ω, 5%, 1/10 W, Automotive, AEC-Q200, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
19	1	R7	RES, 47 kΩ, 5%, 1/10 W, Automotive, AEC-Q200, Thick Film, 0603	ERJ-3GEYJ473V	Panasonic
20	1	R8	RES, 15 Ω, 5%, 1/8 W, Automotive, AEC-Q200,Thick Film, 0805	ERJ-6GEYJ150V	Panasonic
21	1	RF1	RES, 8.2 Ω, 1 W, 5% , Fusible/Flame Proof Wire Wound	FKN1WSJR-52-8R2	Yageo
22	1	RV1	275 Vac, 8.6 J, 5 mm, RADIAL	S05K275	Epcos
23	1	T1	Bobbin, EE8.3, Horizontal, 6 pins (8.3 mm W x 8.3 mm L x 6.2 mm H)	MCT-EE8.3-10(H3+3P)	Mycoiltech
24	1	U1	LinkSwitch-CV, SO-8C	LNK623DG	Power Integrations

Miscellaneous Parts

Item	Qty	Ref Des	Description	Mfg Part Number	Manufacturer
1	1	L	Test Point, WHT, Miniature THRU-HOLE MOUNT	5002	Keystone
2	2	N, GND	Test Point, BLK, Miniature THRU-HOLE MOUNT	5001	Keystone
3	1	+5V	Test Point, RED, Miniature THRU-HOLE MOUNT	5000	Keystone
4	10mm	INSULATION1	Tubing & Sleeving-Non Shrink, #20 AWG Tubing PTFE For RF1	TFT20-NT	Parker/Texloc (Atlantic Tubing)

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7 Transformer Specification

7.1 *Electrical Diagram*

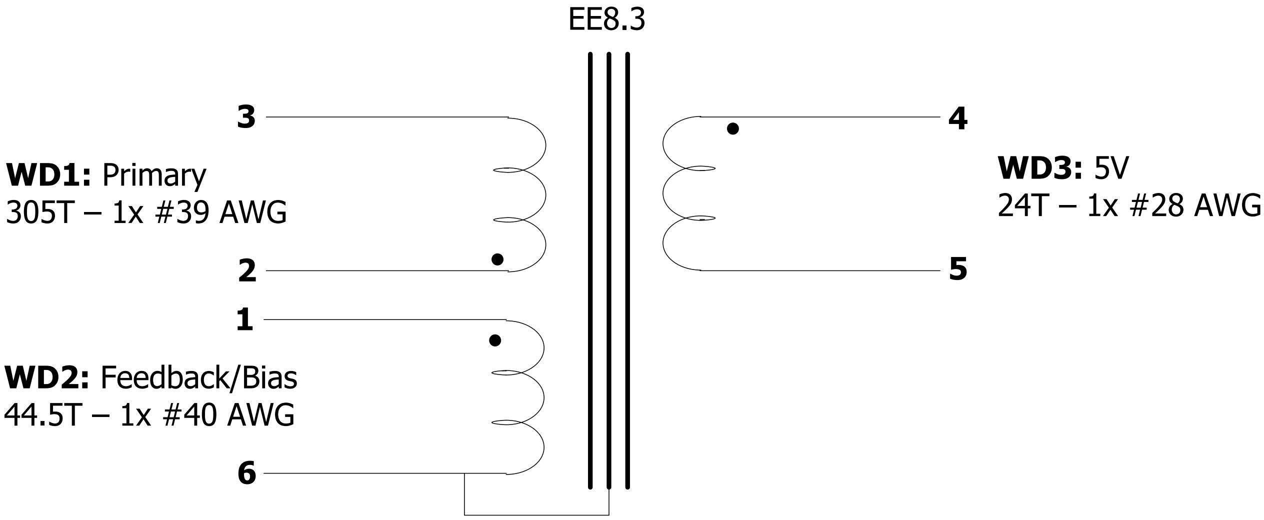

Figure 6 – Transformer Electrical Diagram.

7.2 *Electrical Specification*

Electrical Strength	1 sec, 60 Hz, from pins 2-3 to pins 4-5	3000 VAC
Primary Inductance	Pins 2-3, all other windings open, measured at 100 kHz, 1 V_{RMS}.	1821 μH ±10%
Primary Leakage Inductance	Pins 2-3, with pins 1-6 and pins 4-5 shorted, measured at 100 kHz, 0.4 V_{RMS}.	150 μH (Max.)

7.3 *Material List*

Item	Description
[1]	Core: EE8.3, Ferrite Core PC40, gapped for ALG of 101nH/T².
[2]	Bobbin: EE-8.3 Vertical.
[3]	Magnet Wire: #39 AWG, Double Coated.
[4]	Magnet Wire: #40 AWG, Double Coated.
[5]	Magnet Wire: #28 AWG, Double Coated.
[6]	Tape: 3M 1298 Polyester Film, 1 mil thick, 5 mm Wide.
[7]	Bus Wire: #34 AWG, Belden Electronics Div; or Equivalent.
[8]	Varnish: Dolph BC-359.
[9]	Tape: 3M 1298 Polyester Film 1 mil Thick, 3.5 mm Wide.

7.4 *Transformer Build Diagram*

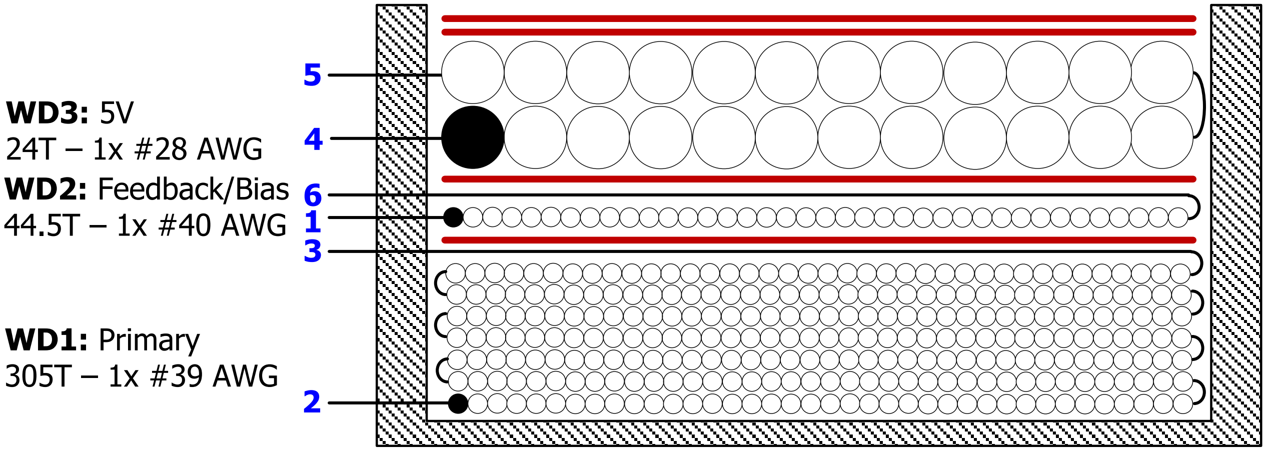

Figure 7 – Transformer Build Diagram.

7.5 *Transformer Instructions*

Winding Preparation	For the purpose of these instructions, bobbin is oriented on winder such that primary side (3-pin) is on the left side with Pin 1 at the upper side. Winding is in clockwise direction.
WD1 Primary	Start at pin 2, wind 305 turns (x1 filar) of wire Item [3] with tight tension. At the last turn, bring the wire back to the left and terminate at pin 3.
Insulation	1 layer of tape Item [6] for insulation.
WD2 Feedback/Bias	Start at pin 1, wind 44.5 turns (x1 filar) of wire Item [4]. Terminate winding at pin 6.
Insulation	1 layer of tape Item [6] for insulation.
WD3 Secondary	Start at pin 4, wind 24 turns (x1 filar) of wire Item [4]. Terminate winding at pin 5.
Insulation	2 layers of tape Item [6] to secure the windings.
Finish	Gap core halves for 1821 μH inductance. Use 1” of bus wire Item [7] solder to pin 3. Wrap core halves and bus wire above which lean along the core with tape Item [9]. Coat with Varnish Item [8].

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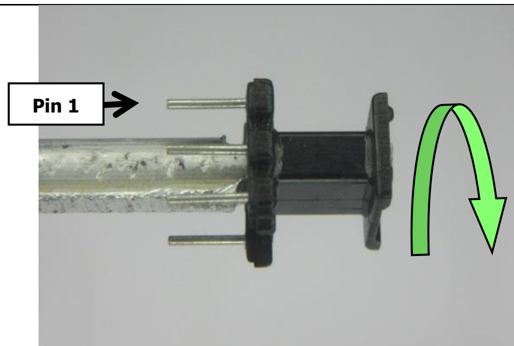
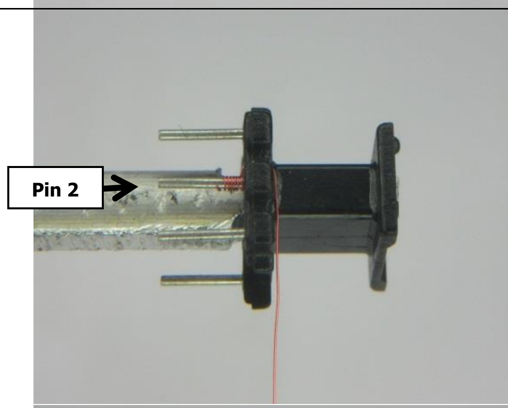
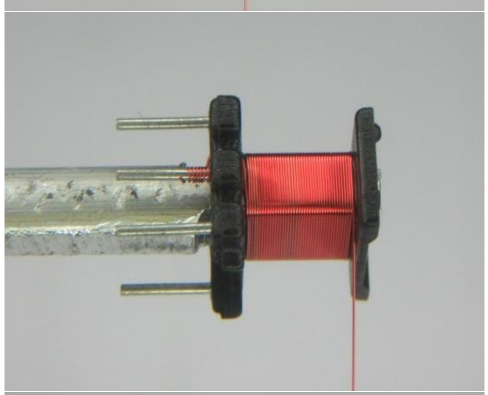
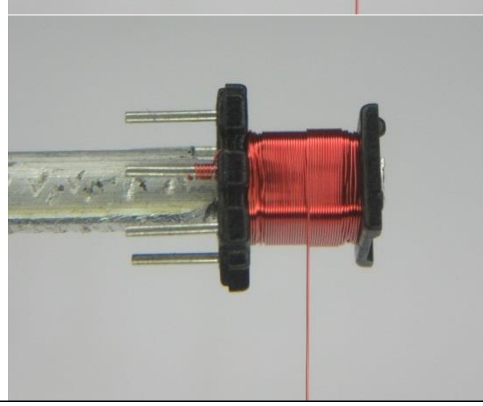
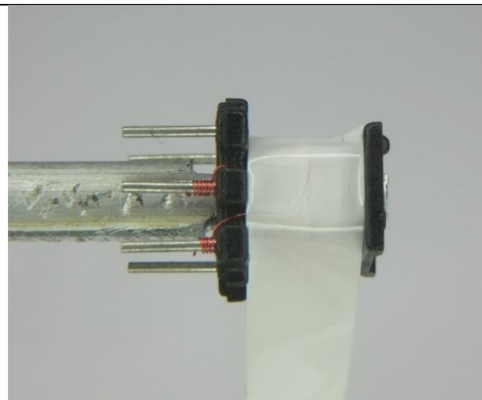
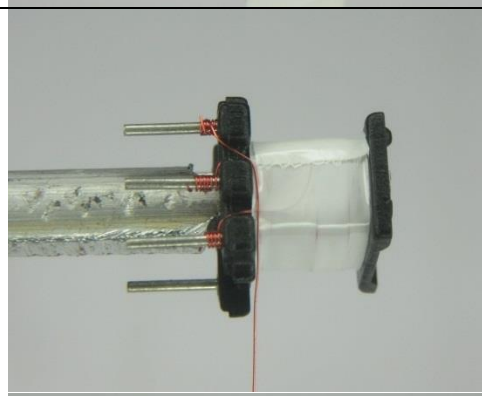
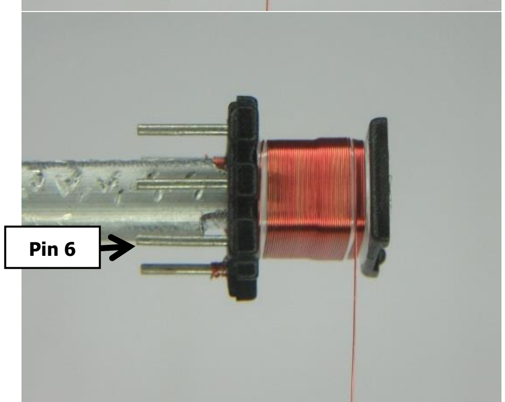
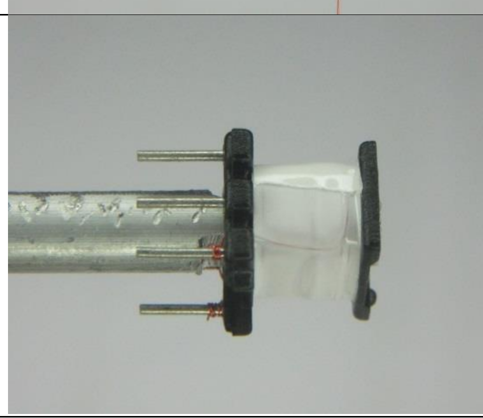
7.6 *Winding Illustrations*

Winding Preparation		For the purpose of these instructions, bobbin is oriented on winder such that primary side (3-pin) is on the left side with Pin 1 at the upper side. Winding is in clockwise direction.
WD1 Primary		Start at pin 2, wind 305 turns (x1 filar) of wire Item [3] with tight tension. At the last turn, bring the wire back to the left and terminate at pin 3.

Insulation		1 layer of tape Item [6] for insulation.
WD2 Feedback/Bias		Start at pin 1, wind 44.5 turns (x1 filar) of wire Item [4].
		Terminate winding at pin 6.
Insulation		1 layer of tape Item [6] for insulation.

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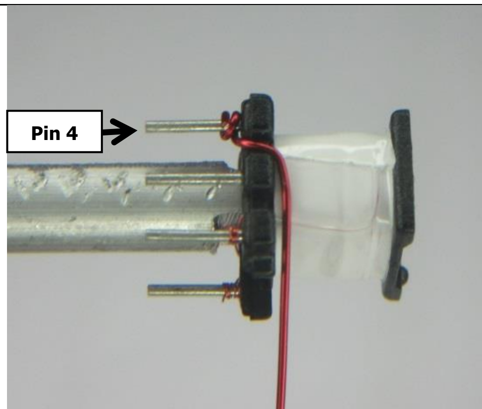
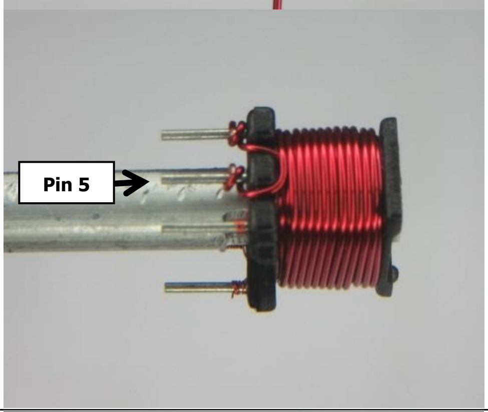
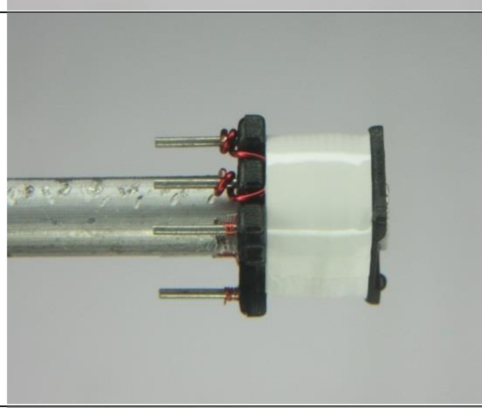
<table>
<tr><td>WD5
Secondary</td><td>


</td><td>Start at pin 4, wind 24 turns (x1 filar) of wire Item [4].

Terminate winding at pin 5.</td></tr>
<tr><td>Insulation</td><td></td><td>2 layers of tape Item [6] to secure the windings.</td></tr>
<tr><td>Finish</td><td></td><td>Gap core halves for 1821 μH inductance.</td></tr>
</table>

Finish	  	Use 1” of bus wire Item [7] solder to pin 6. Wrap core halves and bus wire above which lean along the core with tape Item [9]. Coat with varnish Item [8].

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8 Design Spreadsheet

1	ACDC_LNK-CV_010716; Rev.1.21; Copyright Power Integrations 2015	INPUT	INFO	OUTPUT	UNIT	ACDC_LNK-CV_010716_Rev1-21.xls; LinkSwitch-CV Continuous/Discontinuous Flyback Transformer Design Spreadsheet
2	**ENTER APPLICATION VARIABLES**					
3	VACMIN	85			Volts	Minimum AC Input Voltage
4	VACMAX	265			Volts	Maximum AC Input Voltage
5	fL	50			Hertz	AC Mains Frequency
6	VO	5.00			Volts	Output Voltage
7	PO	2.50			Watts	Output Power
8	N	0.63				Efficiency Estimate
9	Z			0.50		Loss Allocation Factor
10	tC			3.00	mSeconds	Bridge Rectifier Conduction Time Estimate
11	CIN	4.70			uFarads	Input Filter Capacitor
14	**ENTER LinkSwitch-CV VARIABLES**					
15	LinkSwitch-CV	LNK623D		LNK623D		Chosen LinkSwitch-CV device
16	ILIMITMIN			0.196	Amps	LinkSwitch-CV Minimum Current Limit
17	ILIMITMAX			0.225	Amps	LinkSwitch-CV Maximum Current Limit
18	fS			100000	Hertz	LinkSwitch-CV Switching Frequency
19	I2FMIN			3969	A^2Hz	LinkSwitch-CV Min I2F (power Coefficient)
20	I2FMAX			5160	A^2Hz	LinkSwitch-CV Max I2F (power Coefficient)
21	VOR	70		70	Volts	Reflected Output Voltage
22	VDS			10	Volts	LinkSwitch-CV on-state Drain to Source Voltage
23	VD			0.5	Volts	Output Winding Diode Forward Voltage Drop
24	DCON			4.59	us	Output Diode conduction time
25	KP_TRANSIENT			1.11		Worst case ripple to peak current ratio. Maintain KP_TRANSIENT above 0.25
27	**ENTER TRANSFORMER CORE/CONSTRUCTION VARIABLES**					
28	Core Type	Auto		EE8.3		Transformer Core size
29	Core		EE8.3		P/N:	
30	Bobbin		EE8.3 Vertical		P/N:	EE8.3
31	AE	0.07		0.07	cm^2	Core Effective Cross Sectional Area
32	LE	1.9		1.9	cm	Core Effective Path Length
33	AL	610		610	nH/T^2	Ungapped Core Effective Inductance
34	BW	4.7		4.7	mm	Bobbin Physical Winding Width
35	M	0.00		0.00	mm	Safety Margin Width (Half the Primary to Secondary Creepage Distance)
36	L			3		Number of Primary Layers
37	NS	24		24		Number of Secondary Turns
39	**DC INPUT VOLTAGE PARAMETERS**					
40	VMIN	70		70	Volts	Minimum DC Input Voltage
41	VMAX			375	Volts	Maximum DC Input Voltage
43	**FEEDBACK VARIABLES**					
44	NFB	44.00		44.00		Feedback winding number of turns
45	VFLY			10.08	Volts	Voltage on the Feedback winding when LinkSwitch-CV turns off
46	RUPPER			20.00	k-ohms	Upper resistor of feedback network
47	RLOWER			4.53	k-ohms	Lower resistor of feedback network
48	Fine Tuning Section					
49	Measured Output Voltage			5.00	Volts	Actual (Measured) Voltage at the output of power supply
50	RLOWER_FINE			4.64	k-ohms	Adjusted (Fine tuned) value of lower resistor (RLOWER). Do not change value of RUPPER
53	Bias Winding Parameters					

54	Add Bias winding			NO		Bias winding is not necessary. The feedback winding itself can be used as a bias winding
55	VB			N/A	Volts	Bias Winding Voltage
56	NB			N/A		Number of Bias winding turns. Bias winding is assumed to be AC stacked on top of the Feedback winding
57	REXT			N/A	k-ohm	Suggested value of BYPASS pin resistor (use standard 5% resistor)
59	**CURRENT WAVEFORM SHAPE PARAMETERS**					
60	DMAX			0.54		Maximum Duty Cycle
61	IAVG			0.06	Amps	Average Primary Current
62	IP			0.20	Amps	Minimum Peak Primary Current
63	IR			0.18	Amps	Primary Ripple Current
64	IRMS			0.09	Amps	Primary RMS Current
67	**TRANSFORMER PRIMARY DESIGN PARAMETERS**					
68	LPMIN			1639	uHenries	Minimum Primary Inductance
69	LP_TYP			1821	uHenries	Typical (Nominal) Primary Inductance
70	LP_TOL	10		10		Tolerance of Primary inductance
71	NP			305		Primary Winding Number of Turns
72	ALG			20	nH/T^2	Gapped Core Effective Inductance
73	BM			1788	Gauss	Maximum Flux Density, (BM<2500) Calculated at typical current limit and typical primary inductance
74	BP			2069	Gauss	Peak Flux Density, (BP<3100) Calculated at maximum current limit and maximum primary inductance
75	BAC			721	Gauss	AC Flux Density for Core Loss Curves (0.5 X Peak to Peak)
76	ur			1318		Relative Permeability of Ungapped Core
77	LG			0.49	mm	Gap Length (Lg > 0.1 mm)
78	BWE			14.1	mm	Effective Bobbin Width
79	OD	0.14		0.14	mm	Maximum Primary Wire Diameter including insulation
80	INS			0.03	mm	Estimated Total Insulation Thickness (= 2 * film thickness)
81	DIA			0.11	mm	Bare conductor diameter
82	AWG			38	AWG	Primary Wire Gauge (Rounded to next smaller standard AWG value)
83	CM			16	Cmils	Bare conductor effective area in circular mils
84	CMA		**TRF Thermals within limits	185	Cmils/Amp	!!! INCREASE CMA>200 (increase L(primary layers),decrease NS,larger Core)
87	**TRANSFORMER SECONDARY DESIGN PARAMETERS**					
88	Lumped parameters					
89	ISP			2.49	Amps	Peak Secondary Current
90	ISRMS			1.02	Amps	Secondary RMS Current
91	IO			0.50	Amps	Power Supply Output Current
92	IRIPPLE			0.89	Amps	Output Capacitor RMS Ripple Current
93	CMS			203	Cmils	Secondary Bare Conductor minimum circular mils
94	AWGS			27	AWG	Secondary Wire Gauge (Rounded up to next larger standard AWG value)
95	DIAS			0.36	mm	Secondary Minimum Bare Conductor Diameter
96	ODS			0.20	mm	Secondary Maximum Outside Diameter for Triple Insulated Wire
97	INSS			-0.08	mm	Maximum Secondary Insulation Wall Thickness
100	**VOLTAGE STRESS PARAMETERS**					
101	VDRAIN			542	Volts	Maximum Drain Voltage Estimate (Includes Effect of Leakage Inductance)
102	PIVB			N/A	Volts	Bias Diode Maximum Peak Inverse Voltage
103	PIVS			34	Volts	Output Rectifier Maximum Peak Inverse Voltage
106	**TRANSFORMER SECONDARY DESIGN PARAMETERS (MULTIPLE OUTPUTS)**					

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107	1st output					
108	VO1			5	Volts	Output Voltage (if unused, defaults to single output design)
109	IO1			0.50	Amps	Output DC Current
110	PO1			2.5	Watts	Output Power
111	VD1			0.50	Volts	Output Diode Forward Voltage Drop
112	NS1			24.00		Output Winding Number of Turns
113	ISRMS1			1.02	Amps	Output Winding RMS Current
114	IRIPPLE1			0.89	Amps	Output Capacitor RMS Ripple Current
115	PIVS1			34	Volts	Output Rectifier Maximum Peak Inverse Voltage
116	CMS1			203	Cmils	Output Winding Bare Conductor minimum circular mils
117	AWGS1			27	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
118	DIAS1			0.36	mm	Minimum Bare Conductor Diameter
119	ODS1			0.20	mm	Maximum Outside Diameter for Triple Insulated Wire
121	2nd output					
122	VO2				Volts	Output Voltage
123	IO2				Amps	Output DC Current
124	PO2			0	Watts	Output Power
125	VD2			0.70	Volts	Output Diode Forward Voltage Drop
126	NS2			3.05		Output Winding Number of Turns
127	ISRMS2			0.00	Amps	Output Winding RMS Current
128	IRIPPLE2			0.00	Amps	Output Capacitor RMS Ripple Current
129	PIVS2			4	Volts	Output Rectifier Maximum Peak Inverse Voltage
131	CMS2			0	Cmils	Output Winding Bare Conductor minimum circular mils
132	AWGS2			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
133	DIAS2			N/A	mm	Minimum Bare Conductor Diameter
134	ODS2			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
136	3rd output					
137	VO3				Volts	Output Voltage
138	IO3				Amps	Output DC Current
139	PO3			0	Watts	Output Power
140	VD3			0.70	Volts	Output Diode Forward Voltage Drop
141	NS3			3.05		Output Winding Number of Turns
142	ISRMS3			0.00	Amps	Output Winding RMS Current
143	IRIPPLE3			0.00	Amps	Output Capacitor RMS Ripple Current
144	PIVS3			4	Volts	Output Rectifier Maximum Peak Inverse Voltage
146	CMS3			0	Cmils	Output Winding Bare Conductor minimum circular mils
147	AWGS3			N/A	AWG	Wire Gauge (Rounded up to next larger standard AWG value)
148	DIAS3			N/A	mm	Minimum Bare Conductor Diameter
149	ODS3			N/A	mm	Maximum Outside Diameter for Triple Insulated Wire
151	Total power			2.5	Watts	Total Output Power
153	Negative Output	N/A		N/A		If negative output exists enter Output number; eg: If VO2 is negative output, enter 2

9 Performance Data

All measurements performed with external room ambient temperature and 60 Hz input for 115 VAC range and 50 Hz for 230 VAC input range.

9.1 *Full Load Efficiency vs. Line*

Soak for 20 minutes and 5 minutes for each line/step.
Measured at 0.5A Full Load

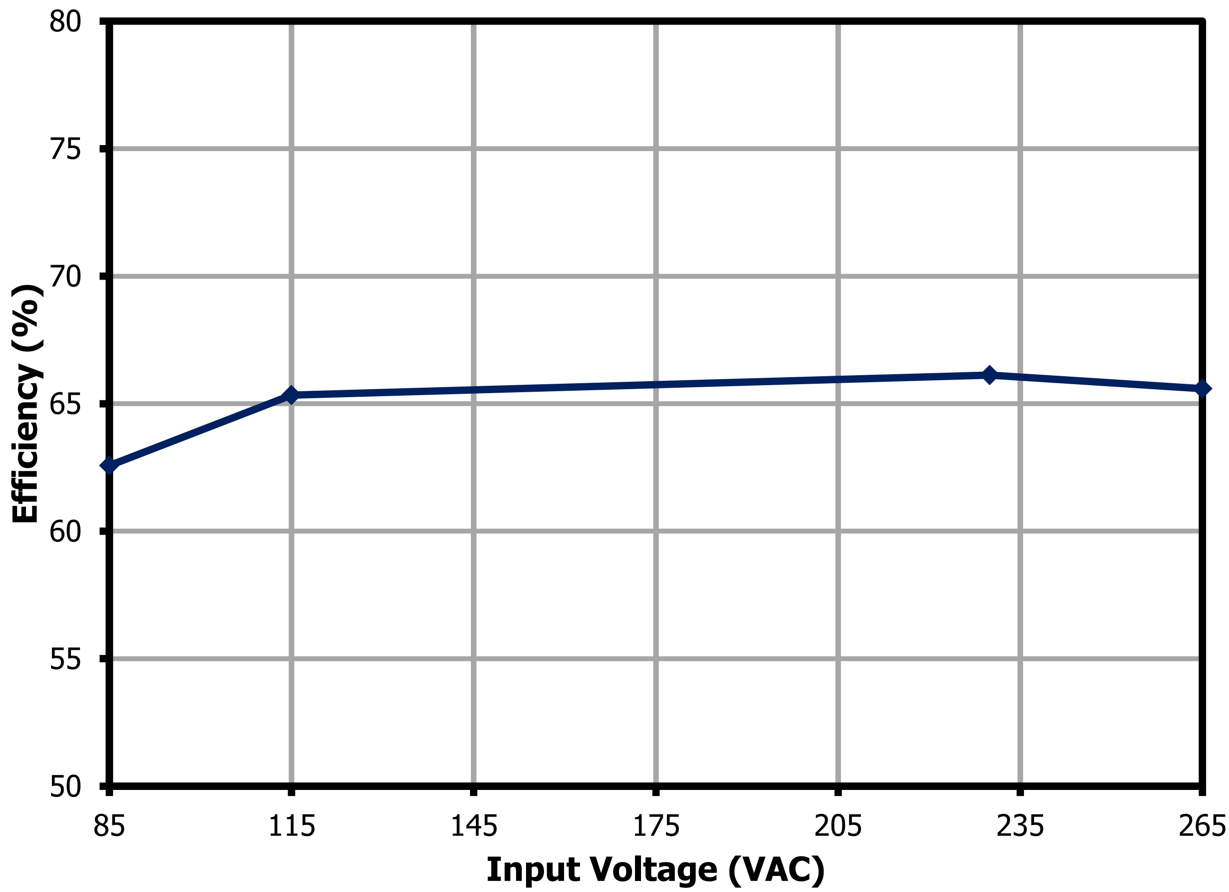

Figure 8 – Efficiency vs. Line.

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9.2 ***Efficiency vs. Load***

Soak for 5 minutes and 30 seconds for each load step.

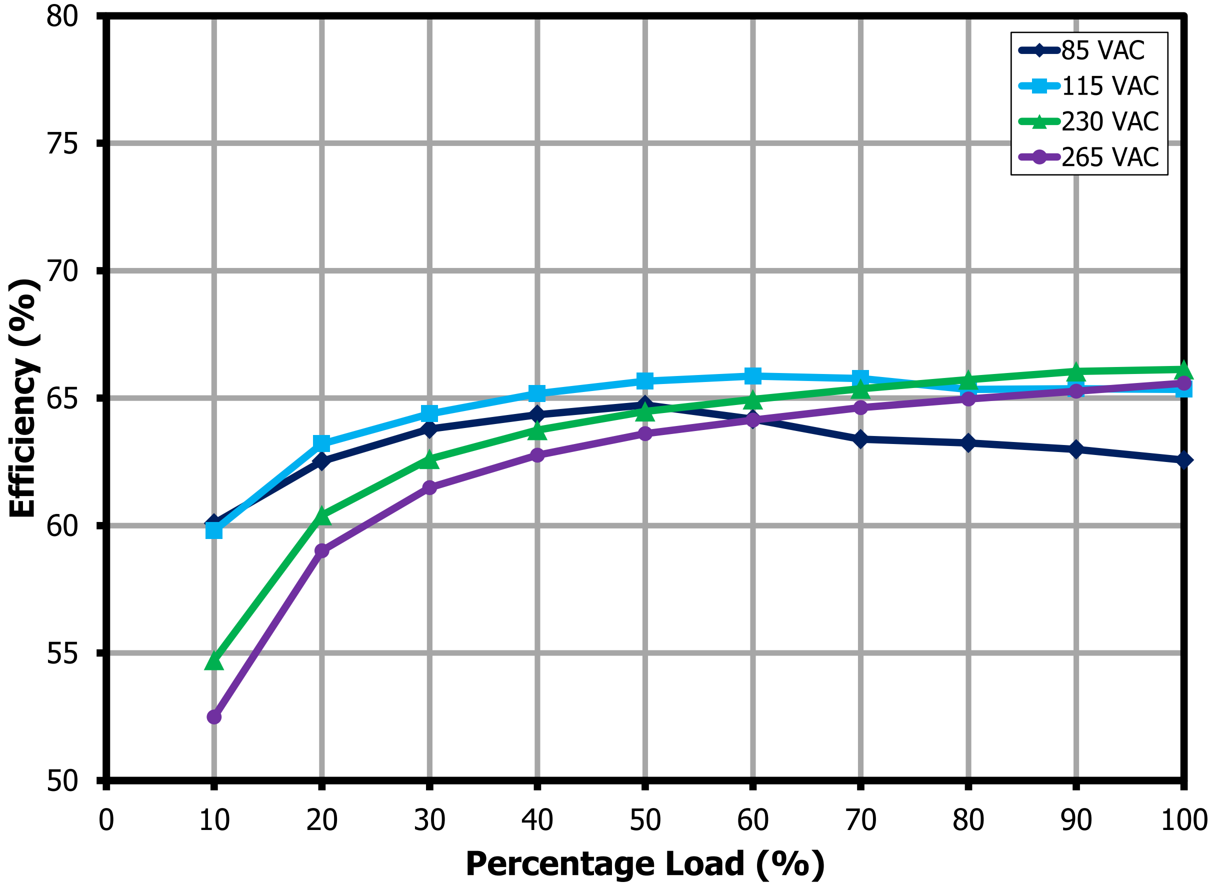

Figure 9 – Efficiency vs. Load (Measured Across PCB Connector).

9.3 *Average Efficiency @ 115 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 6.5 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	114.970	65.160	3.702	4.841	499.760	2.419	65.354
75	114.970	52.780	2.783	4.888	374.780	1.832	65.828
50	114.980	40.510	1.878	4.934	249.930	1.233	65.666
25	114.990	28.040	0.996	5.082	124.970	0.635	63.775
AVERAGE							65.156

9.4 *Average Efficiency @ 230 VAC (PCB End)*

Load Settings	Input Measurement			5 V / 6.5 A Measurement Variable			
% Load	V_{IN} (V_{RMS})	I_{IN} (A_{RMS})	P_{IN} (W)	V_{OUT} (V_{DC})	I_{OUT} (A_{DC})	P_{OUT} (W)	Efficiency (%)
100	229.920	38.490	3.607	4.774	499.690	2.386	66.141
75	229.930	31.550	2.760	4.829	374.760	1.810	65.572
50	229.930	24.220	1.894	4.886	249.910	1.221	64.472
25	229.930	16.001	0.994	4.902	124.960	0.613	61.630
AVERAGE							64.454

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10 No-Load Input Power

Soak for 15 minutes and 3 minutes integration time for each line/step.

Note: Output voltage was clamped using a resistor-Zener diode network (68 Ω and BZT52C47 Zener diode)

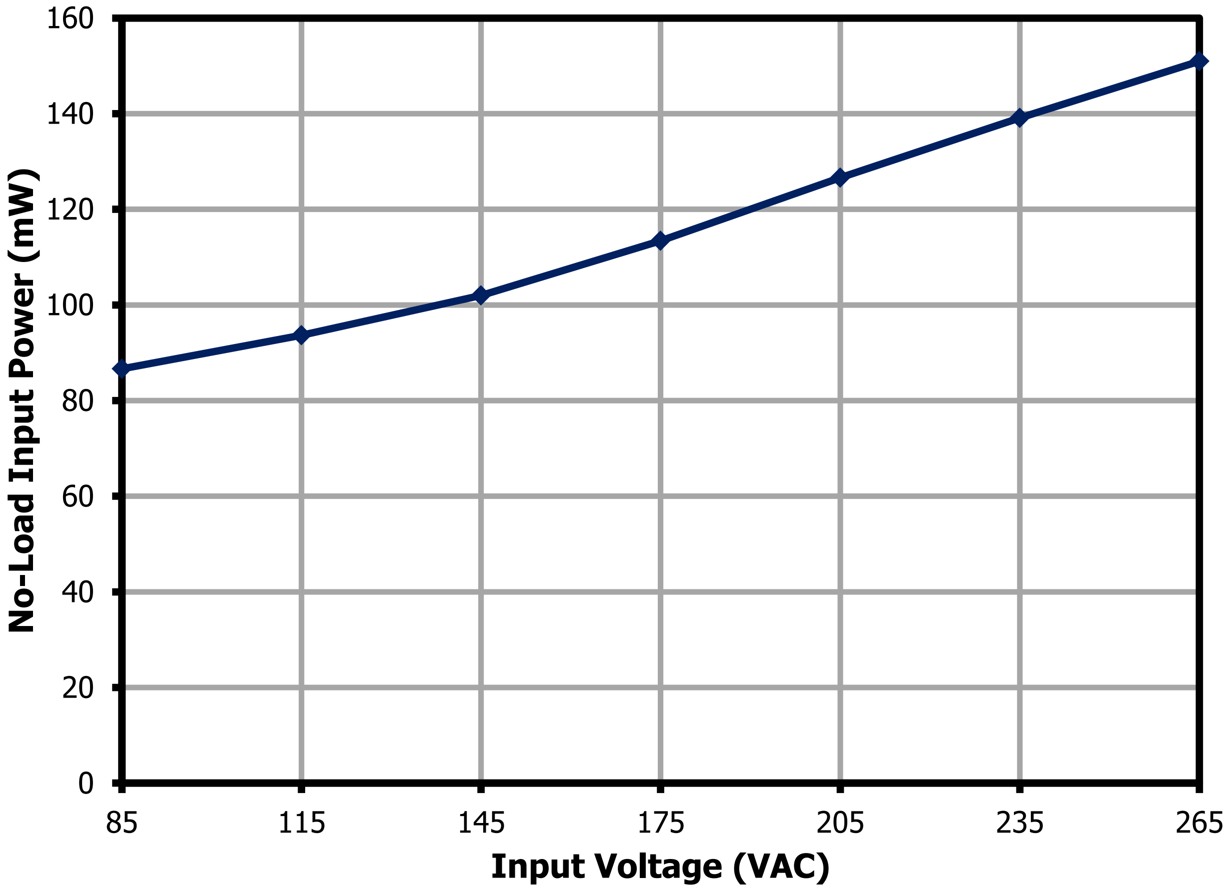

Figure 10 – No-Load Input Power vs. Input Line Voltage, Room Temperature.

11 Line Regulation

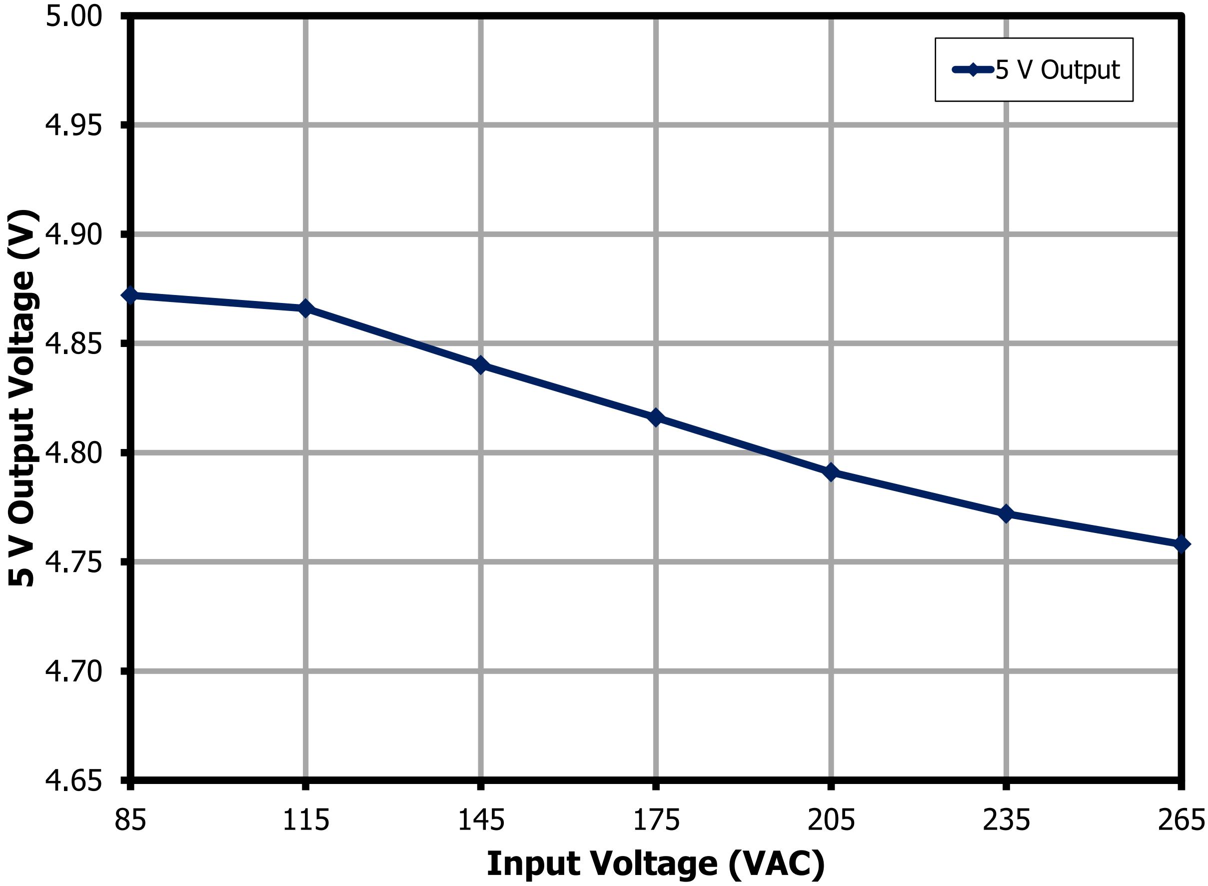

Figure 11 – Full Load Line Regulation

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12 Load Regulation

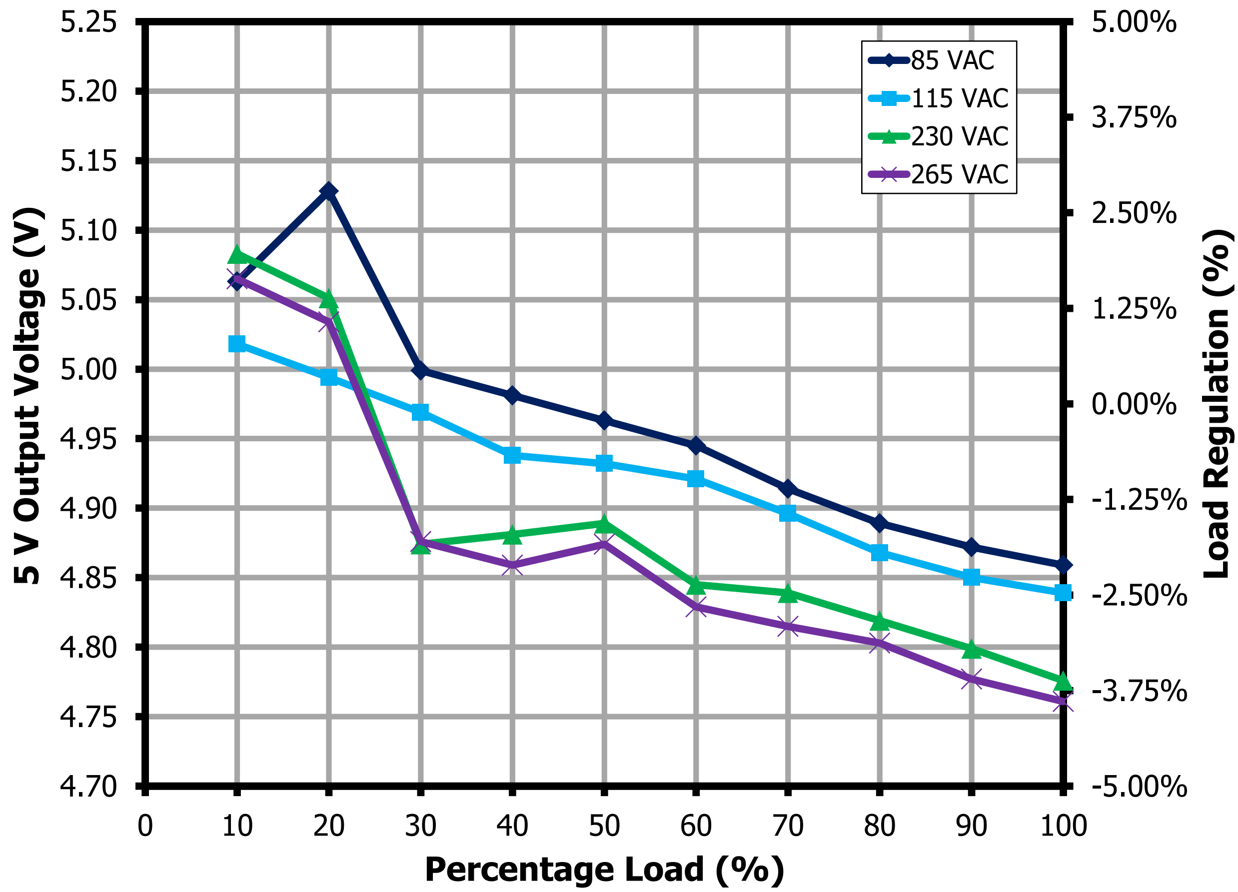

Figure 12 – Load Regulation (Across PCB Connector).

13 Thermal Performance

13.1 *Thermal Scan at Room Temperature*

Open frame unit was placed inside the enclosure to prevent airflow that may affect the thermal measurements. Temperature was measured using Thermal Camera. Soak time at full load is 2 hours.

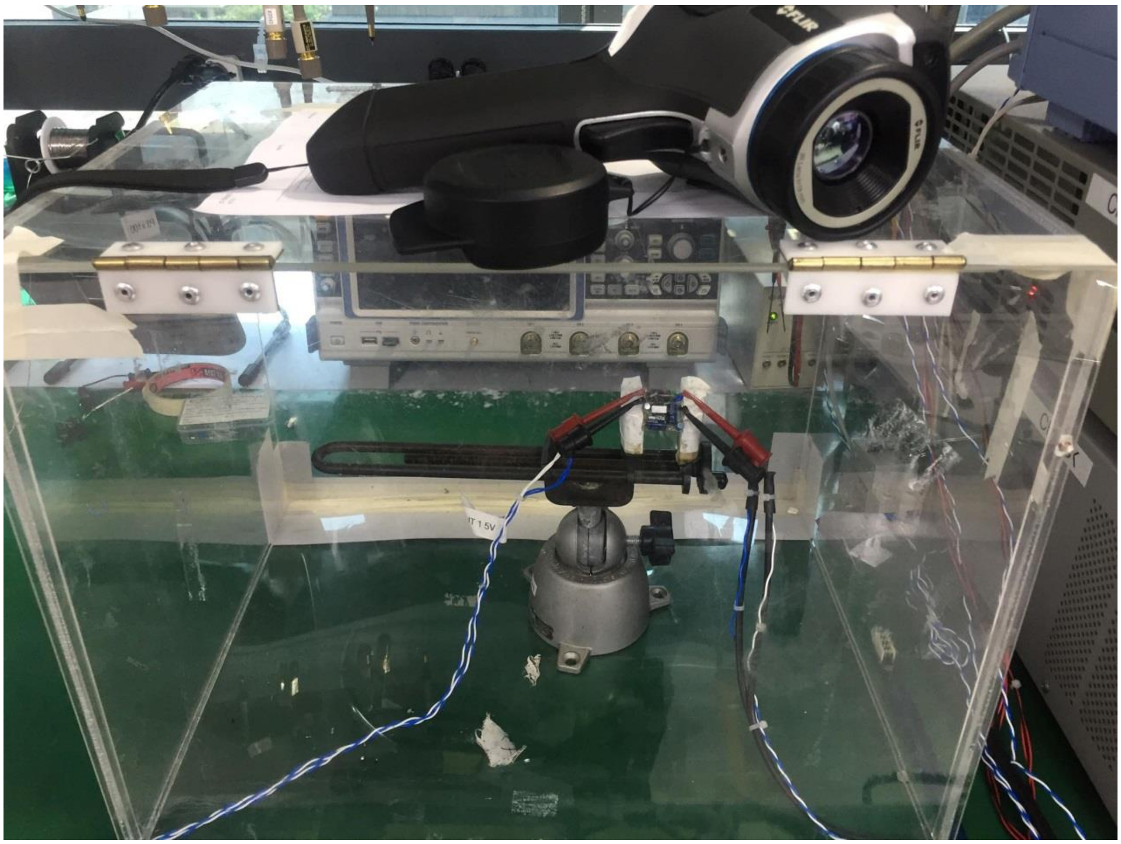

Figure 13 – Test Set-up.

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13.1.1 85 VAC

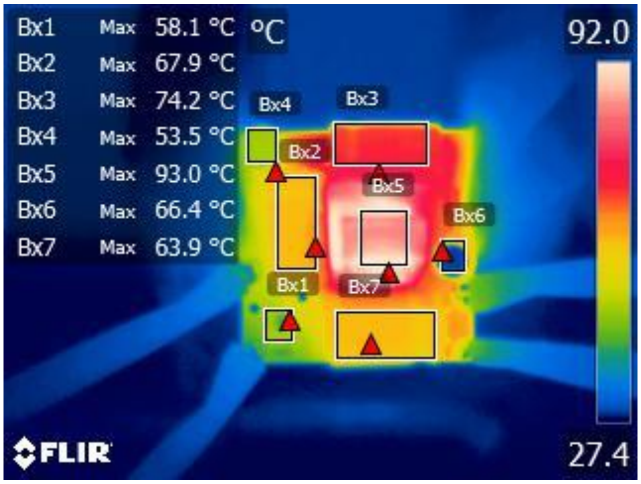

Figure 14 – 85 VAC, 0.5 A Load. Top Side. Ambient = 27.5 ºC.

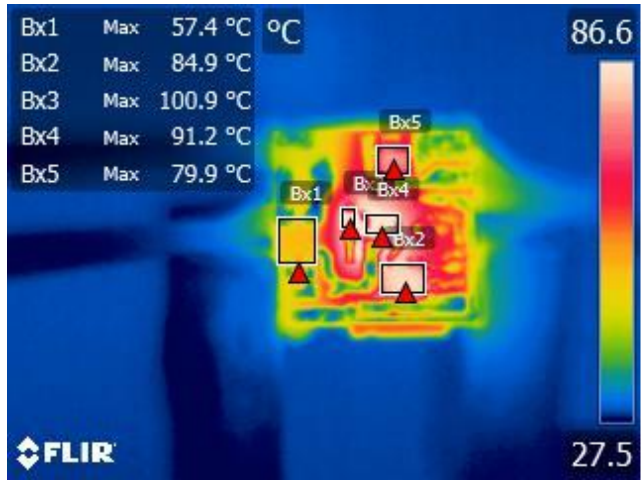

Figure 15 – 85 VAC, 0.5 A Load. Bottom Side. Ambient = 27.5 ºC.

Component	Temperature (°C)
LNK623D (U1)	84.9
Fusible Resistor (RF1)	58.1
Input Capacitor (C1)	67.9
Input Capacitor (C2)	74.2
Input Choke (L1)	53.5
Transformer (T1)	93
Bias Capacitor (C3)	66.4
Output Capacitor (C8)	63.9
Bridge Rectifier (BR1)	57.4
Primary Clamp Diode (D3)	91.2
Primary Clamp Resistor (R2)	100.9
Output Diode (D4)	79.9

13.1.2 265 VAC

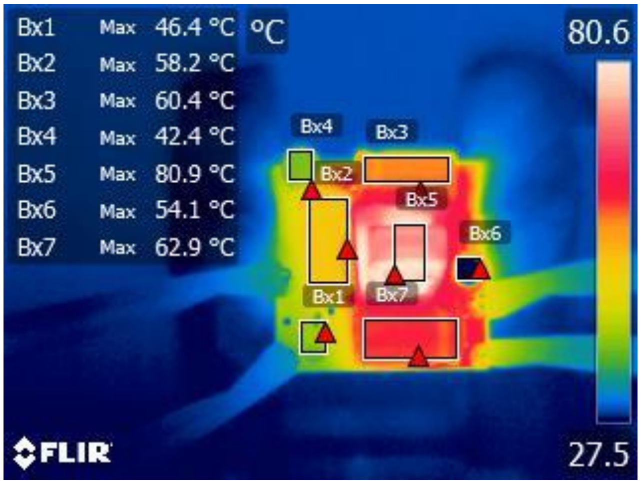

Figure 16 – 265 VAC, 0.5 A Load. Top Side. Ambient = 27.5 ºC.

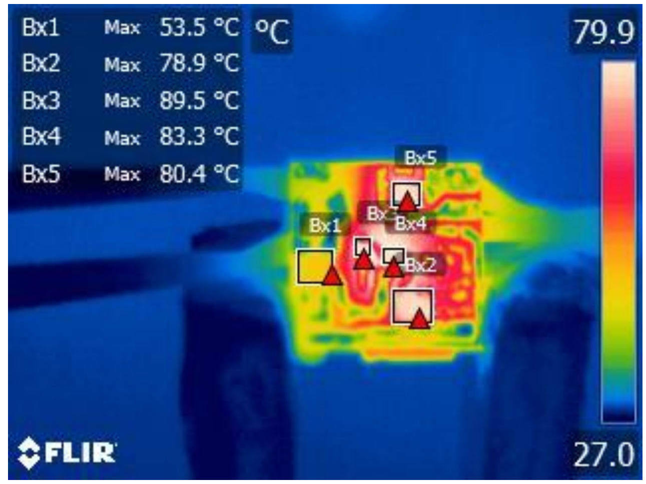

Figure 17 – 265 VAC, 0.5 A Load. Bottom Side. Ambient = 27.5 ºC.

Component	Temperature (ºC)
LNK623D (U1)	78.9
Fusible Resistor (RF1)	46.4
Input Capacitor (C1)	58.2
Input Capacitor (C2)	60.4
Input Choke (L1)	42.4
Transformer (T1)	80.9
Bias Capacitor (C3)	54.1
Output Capacitor (C8)	62.9
Bridge Rectifier (BR1)	53.5
Primary Clamp Diode (D3)	83.3
Primary Clamp Resistor (R2)	89.5
Output Diode (D4)	80.4

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14 Test Waveforms

14.1 *Load Transient Response*

14.1.1 10% - 100% Load Condition 1 kHz 50% duty

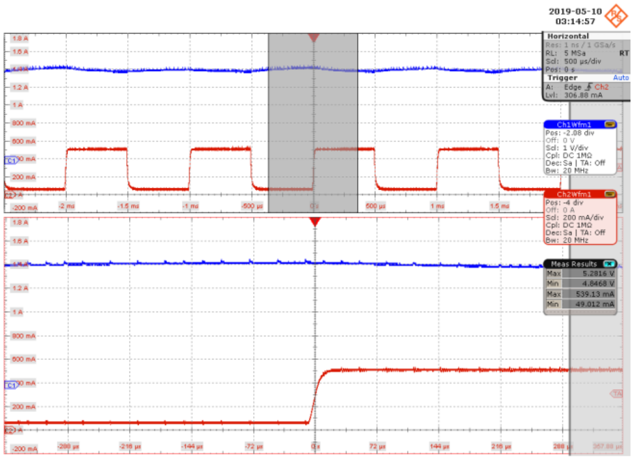

Figure 18 – 85 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 500 µs / div.
CH2: I_{LOAD}, 200 mA / div., 500 µs / div.
Zoom: 72 µs / div.
V_{MAX}: 5.28 V, V_{MIN}: 4.85 V.

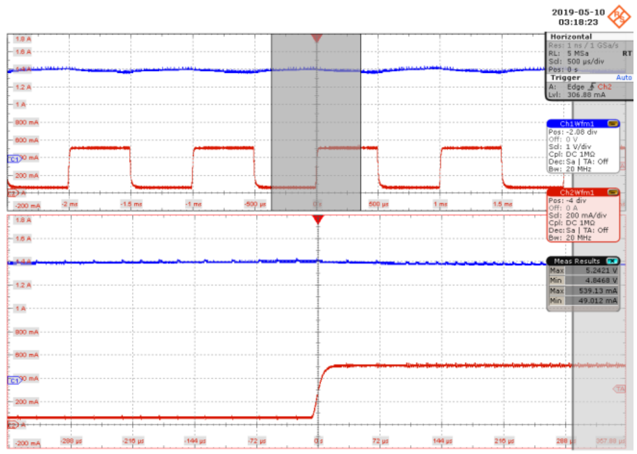

Figure 19 – 115 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 500 µs / div.
CH2: I_{LOAD}, 200 mA / div., 500 µs / div.
Zoom: 72 µs / div.
V_{MAX}: 5.24 V, V_{MIN}: 4.85 V.

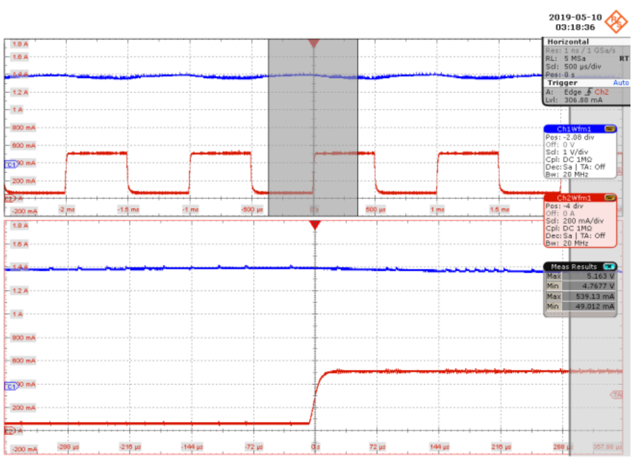

Figure 20 – 230 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 500 µs / div.
CH2: I_{LOAD}, 200 mA / div., 500 µs / div.
Zoom: 72 µs / div.
V_{MAX}: 5.16 V, V_{MIN}: 4.77 V.

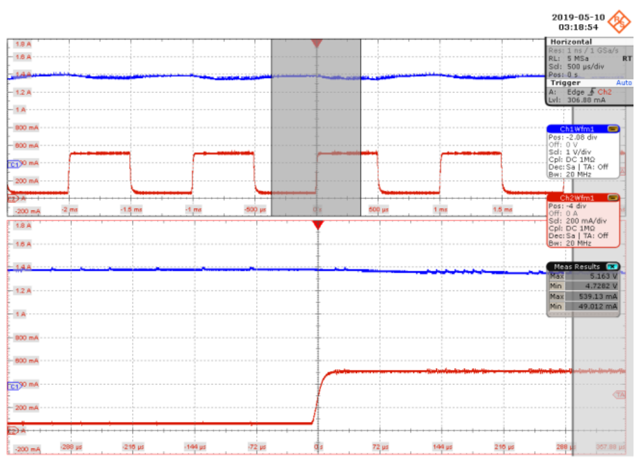

Figure 21 – 265 VAC 60 Hz, 10% - 100% Load.
CH1: V_{OUT}, 1 V / div., 500 µs / div.
CH2: I_{LOAD}, 200 mA / div., 500 µs / div.
Zoom: 72 µs / div.
V_{MAX}: 5.16 V, V_{MIN}: 4.73 V.

14.2 *Output Voltage at Start-up*

14.2.1 CC mode

14.2.1.1 100% Load

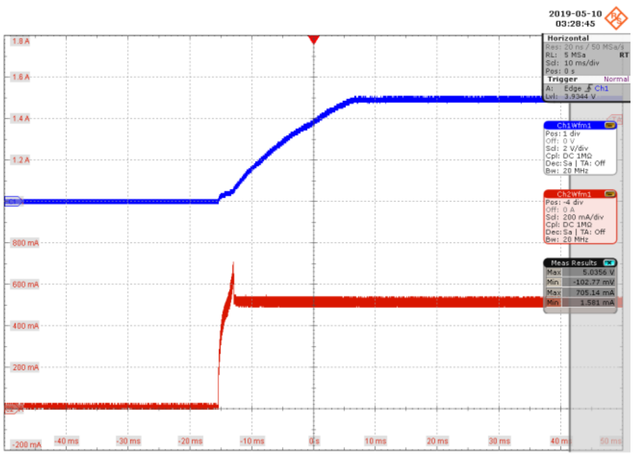

Figure 22 – 85 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 10 ms / div.
Lower: I_{OUT}, 200 mA / div., 10 ms / div.
Output Rise Monotonically.

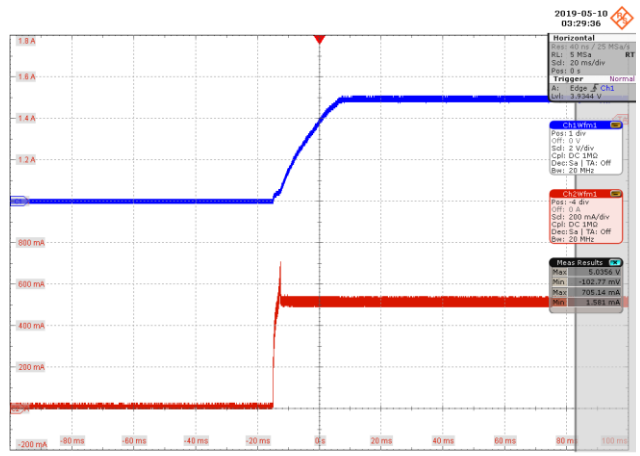

Figure 23 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

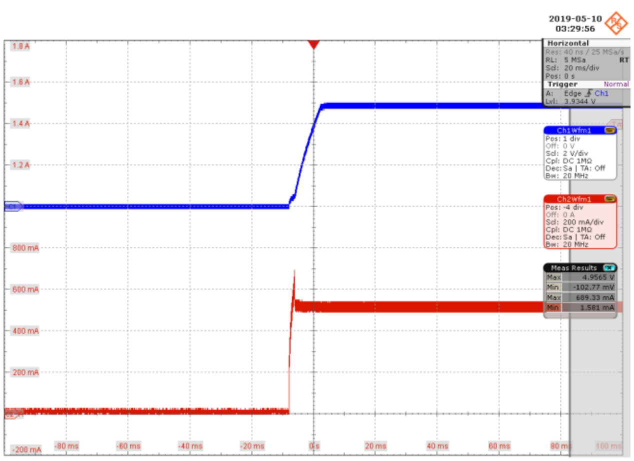

Figure 24 – 230 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

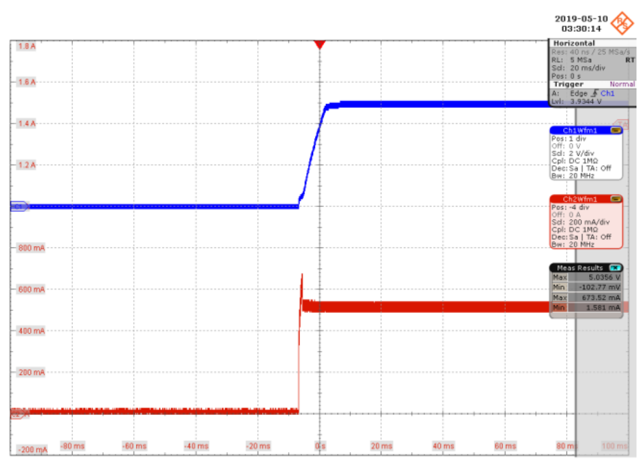

Figure 25 – 265 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

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14.2.1.2 10% Load

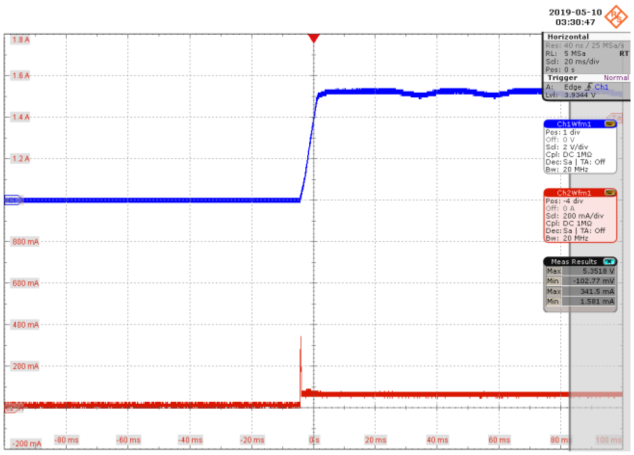

Figure 26 – 85 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

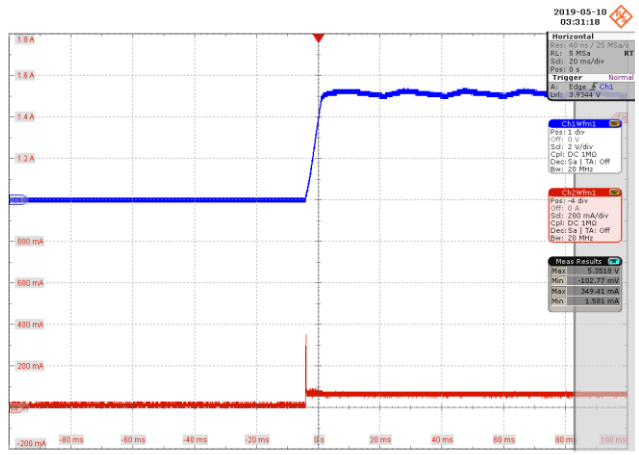

Figure 27 – 115 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

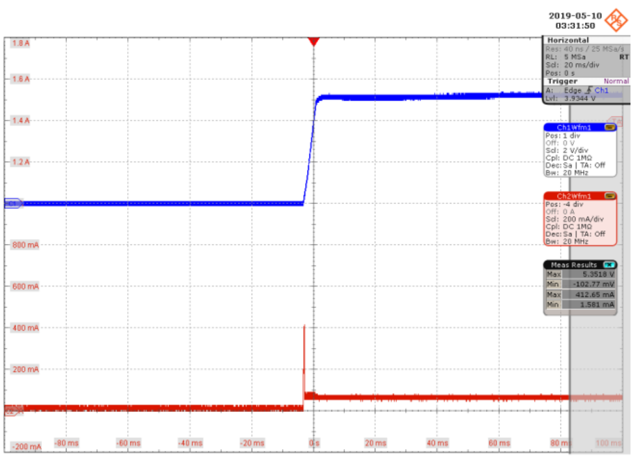

Figure 28 – 230 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

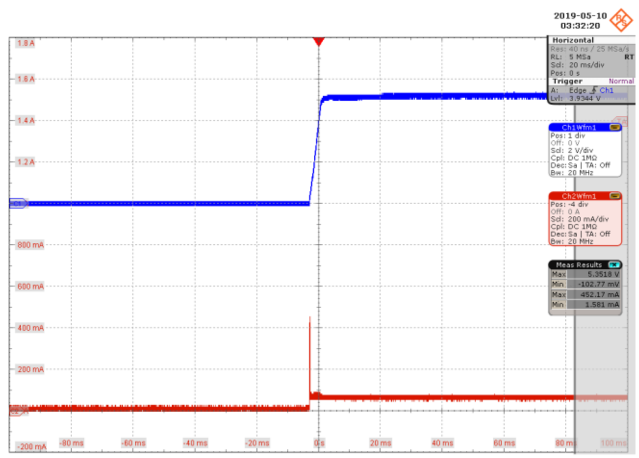

Figure 29 – 265 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

14.2.2 CR mode

14.2.2.1 100% Load

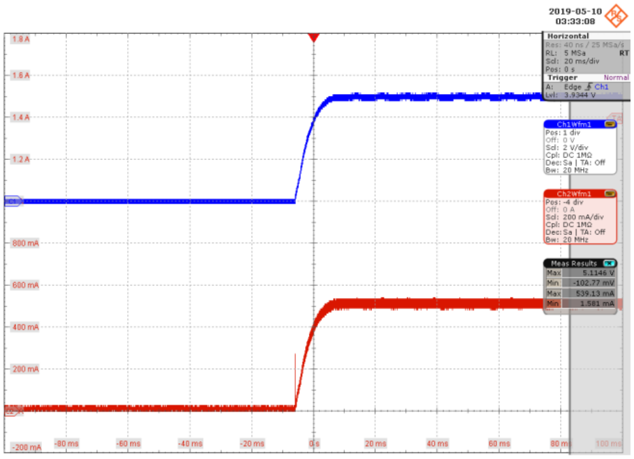

Figure 30 – 85 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

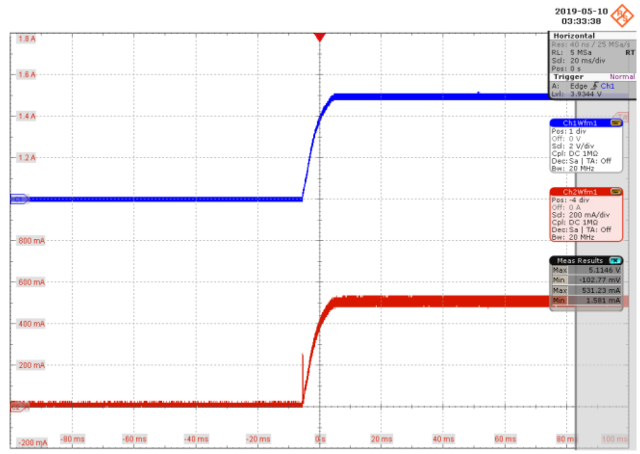

Figure 31 – 115 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

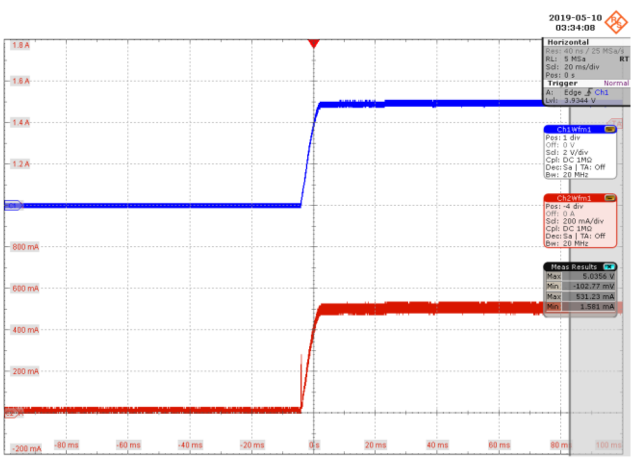

Figure 32 – 230 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

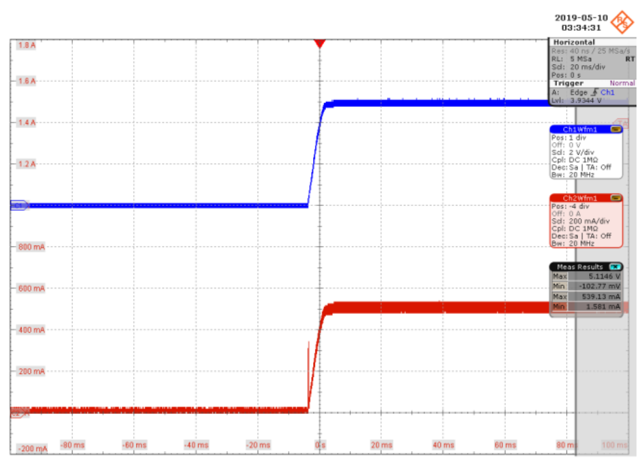

Figure 33 – 265 VAC 60 Hz, Full Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

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14.2.2.2 10% Load

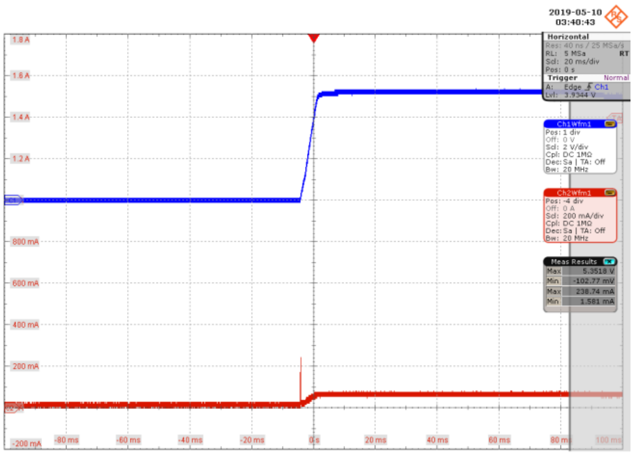

Figure 34 – 85 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

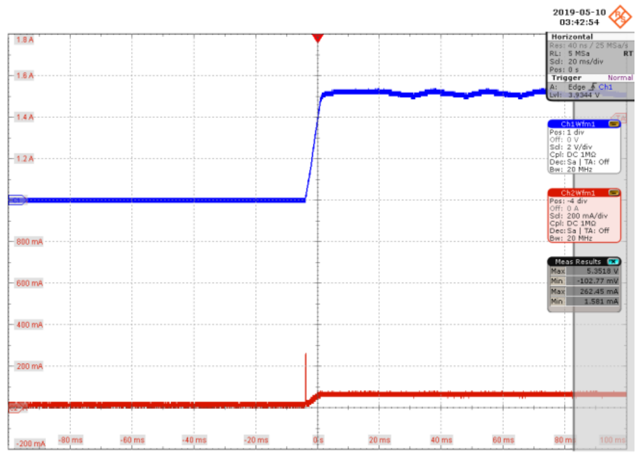

Figure 35 – 115 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

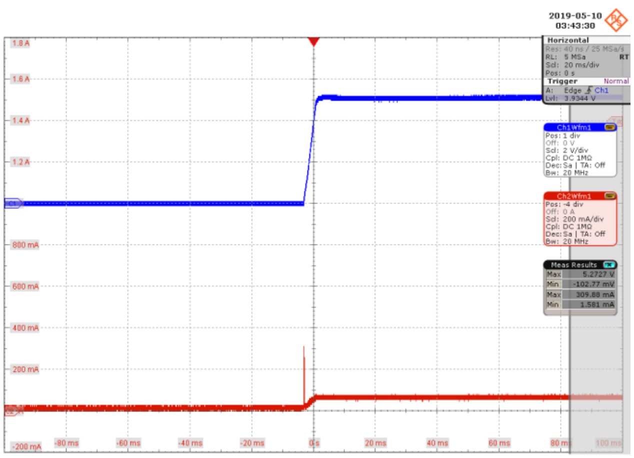

Figure 36 – 230 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

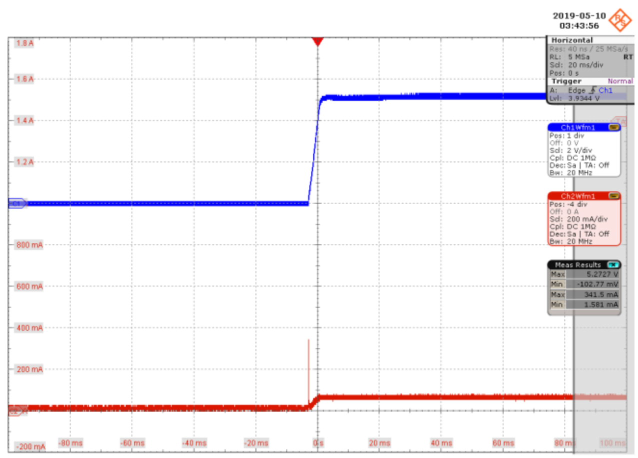

Figure 37 – 265 VAC 60 Hz, Minimum Load Start-up.
Upper: V_{OUT}, 2 V / div., 20 ms / div.
Lower: I_{OUT}, 200 mA / div., 20 ms / div.
Output Rise Monotonically.

14.3 ***Switching Waveforms***

14.3.1 Drain-to-Source Voltage and Current at Normal Operation

14.3.1.1 100% Load

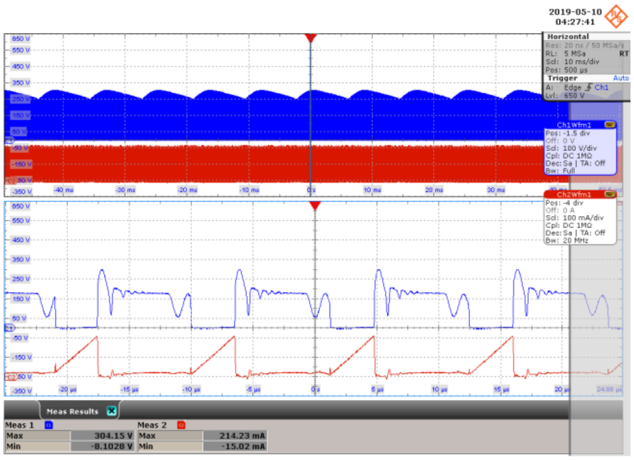

Figure 38 – 85 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 304.15 V, $I_{DS(MAX)}$ = 214.23 mA.

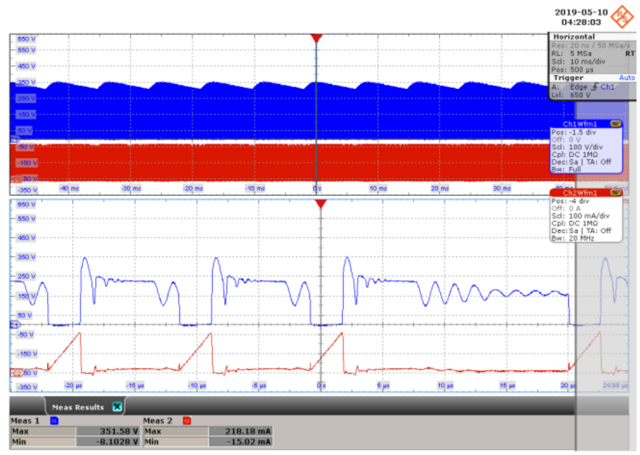

Figure 39 – 115 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 351.58 V, $I_{DS(MAX)}$ = 218.18 mA.

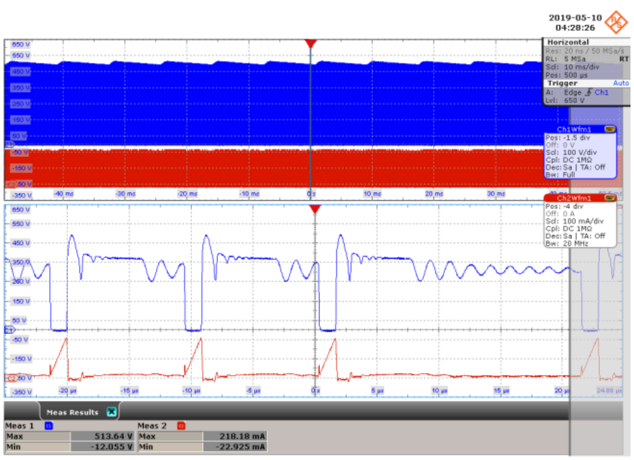

Figure 40 – 230 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 513.64 V, $I_{DS(MAX)}$ = 218.18 mA.

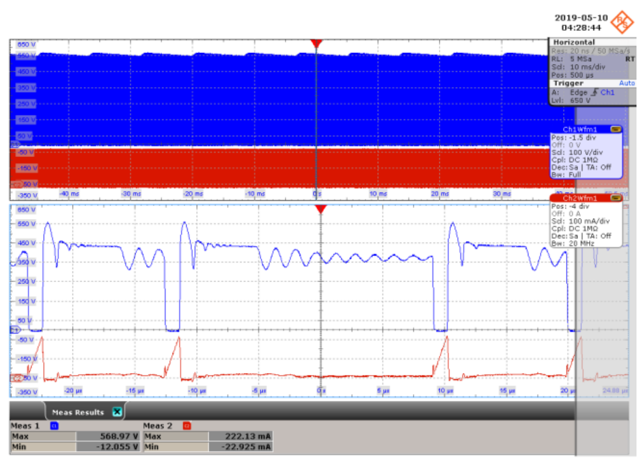

Figure 41 – 265 VAC 60 Hz, Full Load.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 568.97 V, $I_{DS(MAX)}$ = 222.13 mA.

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14.3.1.2 Minimum Load (10% Load)

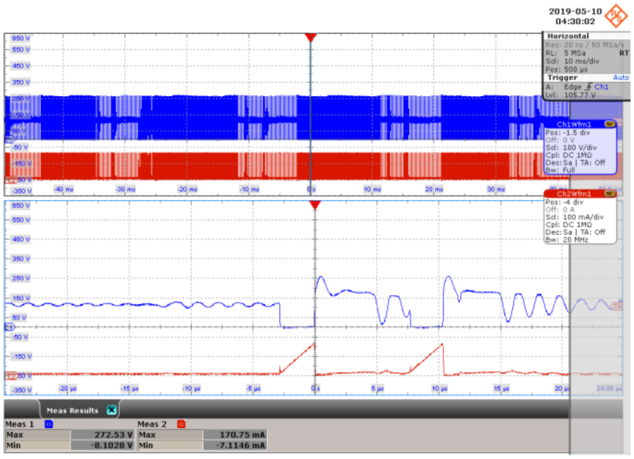

Figure 42 – 85 VAC 60 Hz, Minimum Load
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 272.53 V, $I_{DS(MAX)}$ = 170.75 mA.

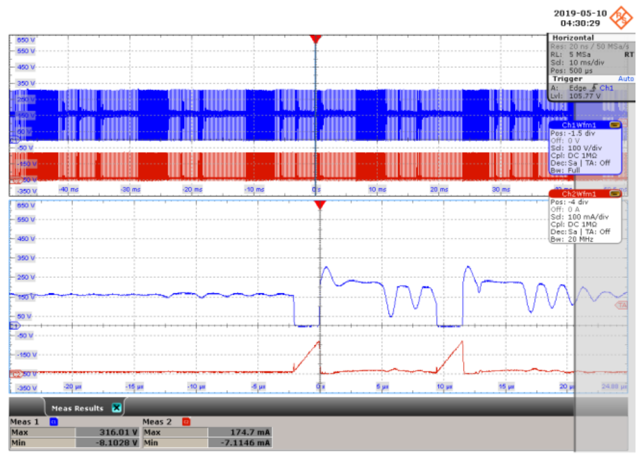

Figure 43 – 115 VAC 60 Hz, Minimum Load
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 316.01 V, $I_{DS(MAX)}$ = 174.7 mA.

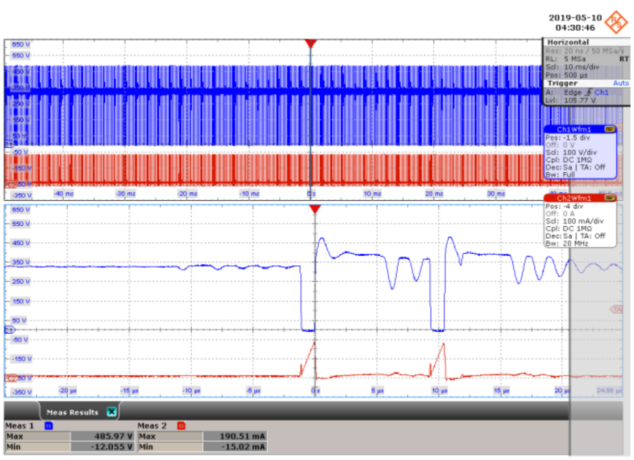

Figure 44 – 230 VAC 60 Hz, Minimum Load
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 485.97 V, $I_{DS(MAX)}$ = 190.51 mA.

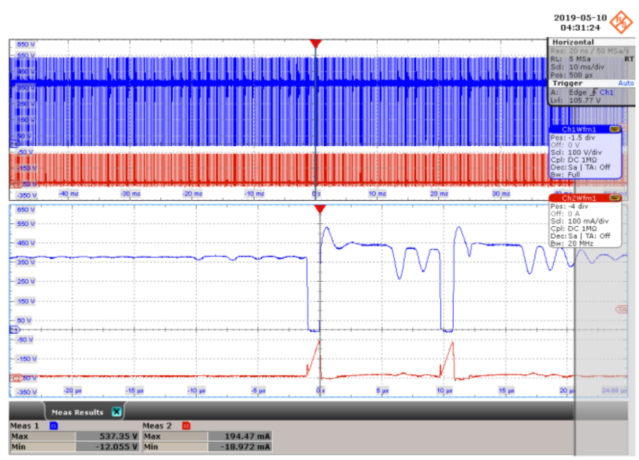

Figure 45 – 265 VAC 60 Hz, Minimum Load
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 537.35 V, $I_{DS(MAX)}$ = 194.47 mA.

14.3.2 Drain-to-Source Voltage and Current at Start-up Operation

14.3.2.1 100% Load

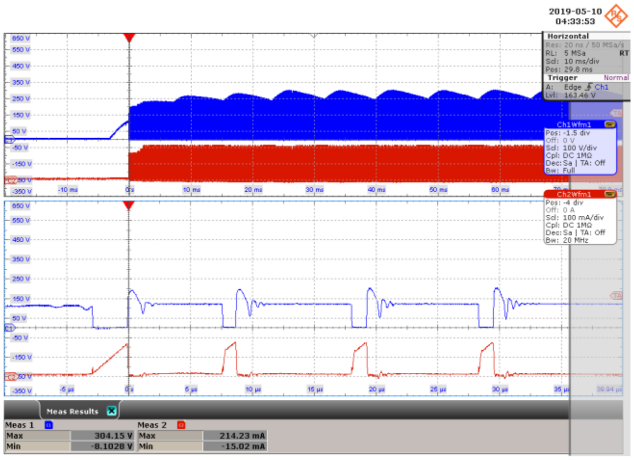

Figure 46 – 85 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 304.15 V, $I_{DS(MAX)}$ = 214.23 mA.

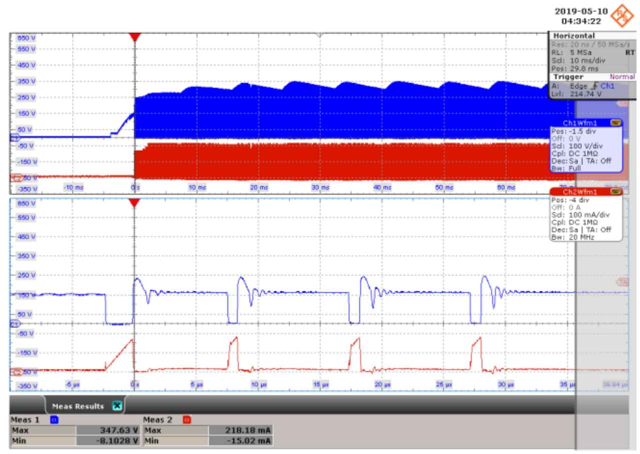

Figure 47 – 115 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 347.63 V, $I_{DS(MAX)}$ = 218.18 mA.

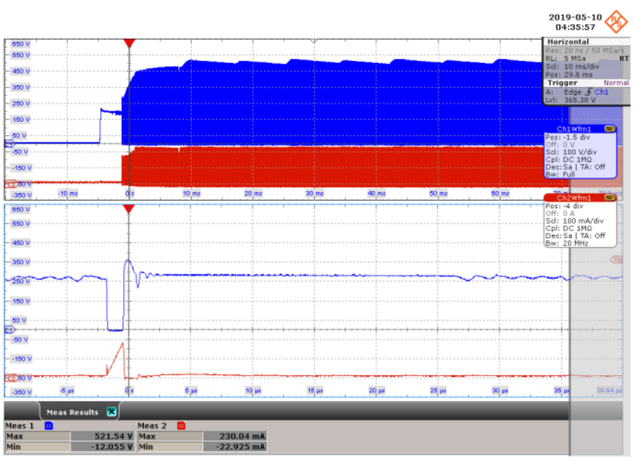

Figure 48 – 230 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 521.54 V, $I_{DS(MAX)}$ = 230.04 mA.

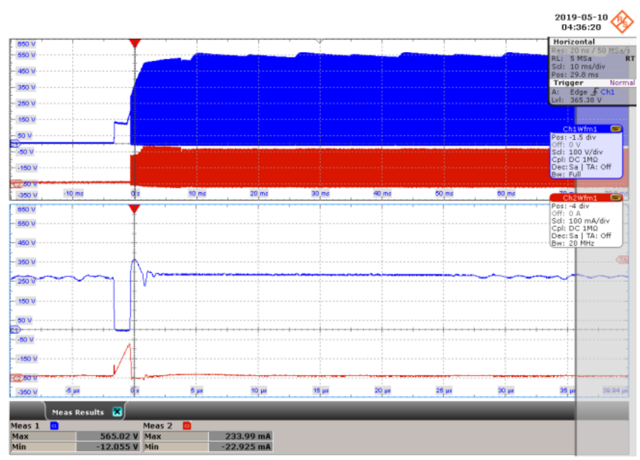

Figure 49 – 265 VAC 60 Hz, Full Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 µs / div.
$V_{DS(MAX)}$ = 565.02 V, $I_{DS(MAX)}$ = 233.99 mA.

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14.3.2.2 Minimum Load (10% Load)

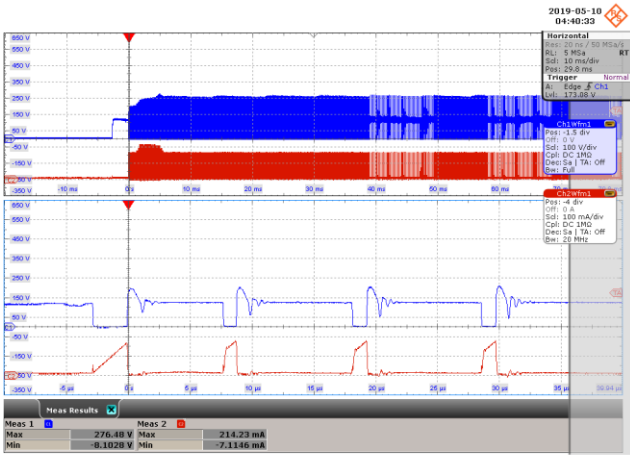

Figure 50 – 85 VAC 60 Hz, Minimum Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 276.48 V, $I_{DS(MAX)}$ = 214.23 mA.

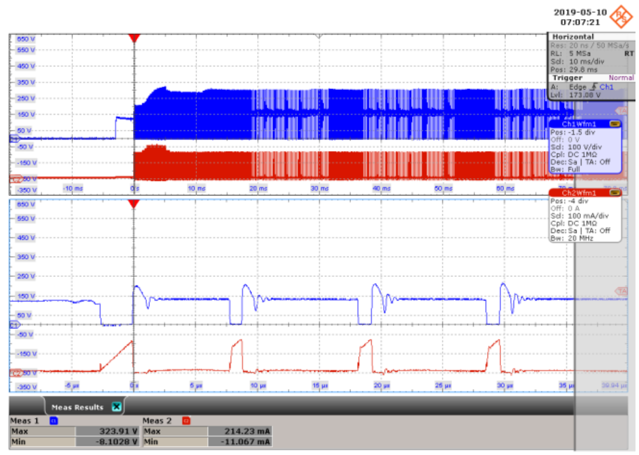

Figure 51 – 115 VAC 60 Hz, Minimum Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 323.91 V, $I_{DS(MAX)}$ = 214.23 mA.

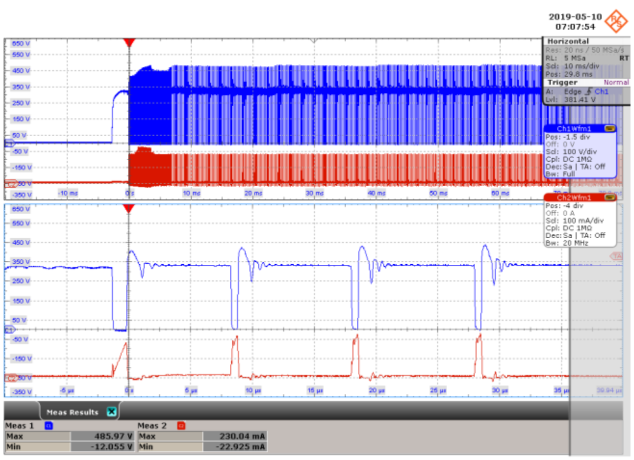

Figure 52 – 230 VAC 50 Hz, Minimum Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 485.97 V, $I_{DS(MAX)}$ = 230.04 mA.

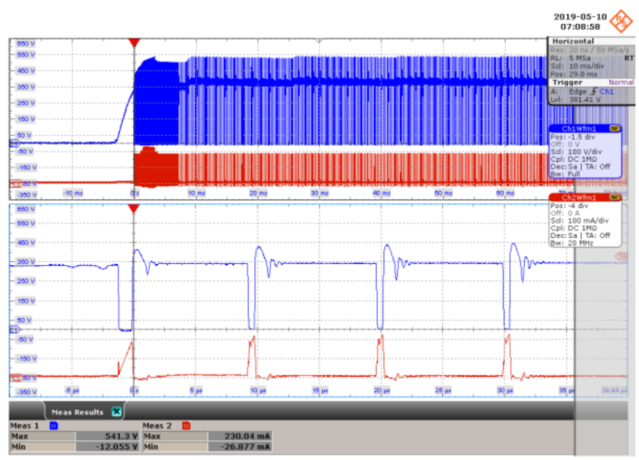

Figure 53 – 265 VAC 50 Hz, Minimum Load Start-up.
CH1: V_{DS}, 100 V / div., 10 ms / div.
CH2: I_{DS}, 100 mA / div., 10 ms / div.
Zoom: 5 μs / div.
$V_{DS(MAX)}$ = 541.3 V, $I_{DS(MAX)}$ = 230.04 mA.

14.3.3 Output Diode Voltage and Current at Normal Operation

14.3.3.1 100% Load

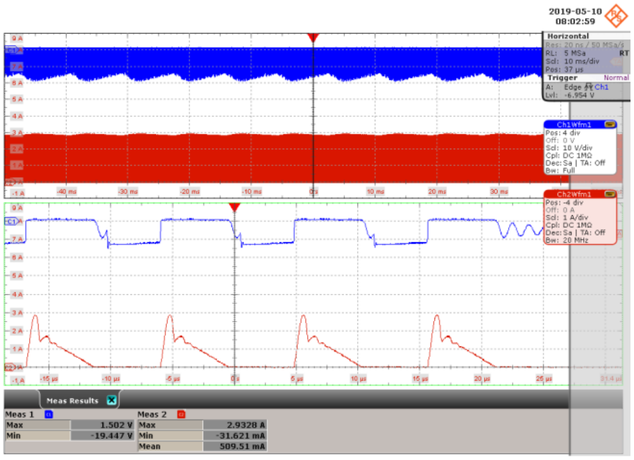

Figure 54 – 85 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 19.45 V.

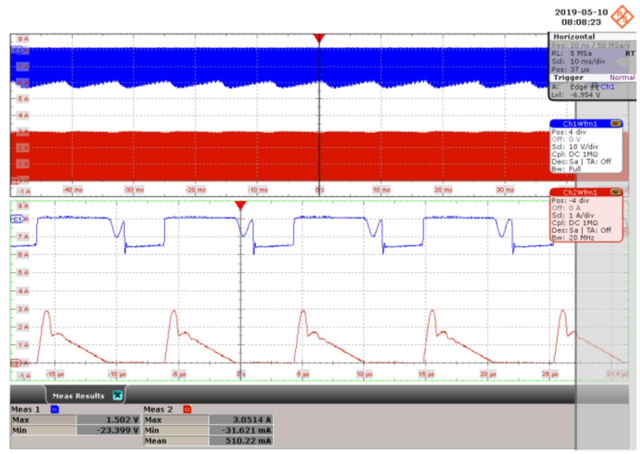

Figure 55 – 115 VAC 60 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 23.40 V.

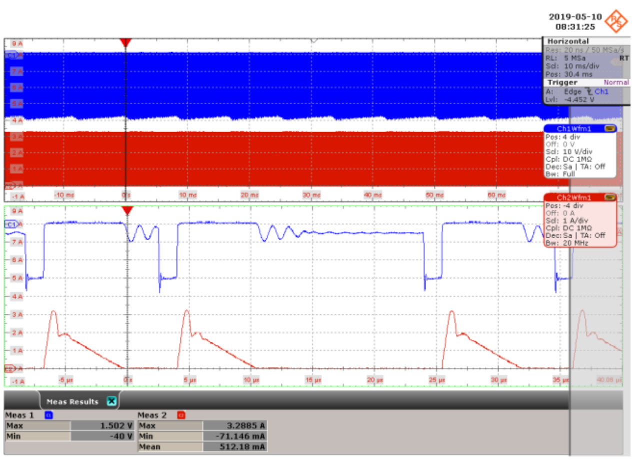

Figure 56 – 230 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 40 V.

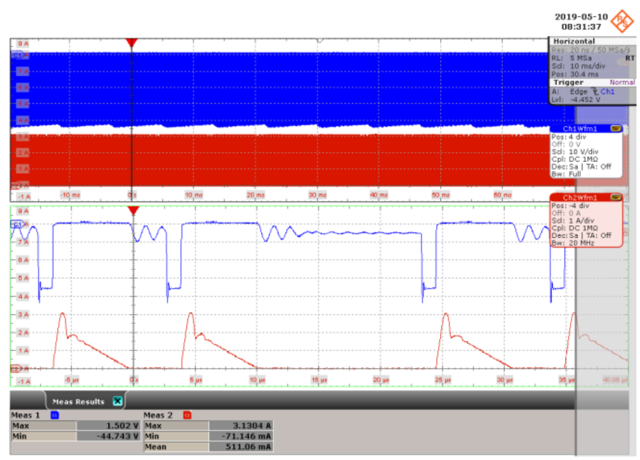

Figure 57 – 265 VAC 50 Hz, Full Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 44.74 V.

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14.3.3.2 10% Load

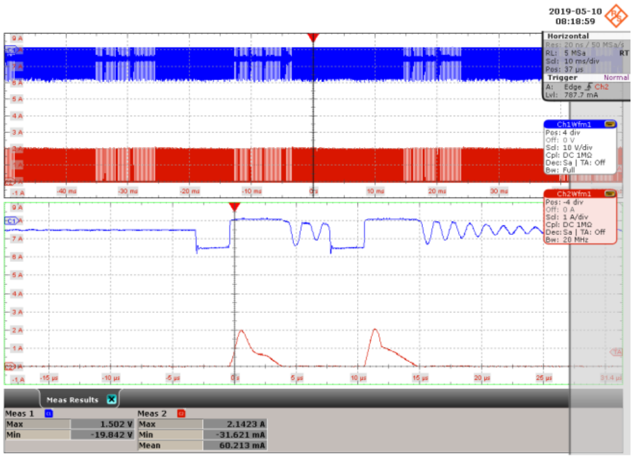

Figure 58 – 85 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 19.84 V.

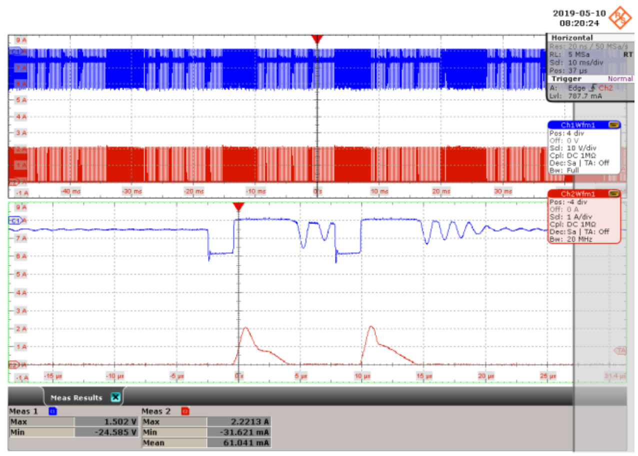

Figure 59 – 115 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 24.59 V.

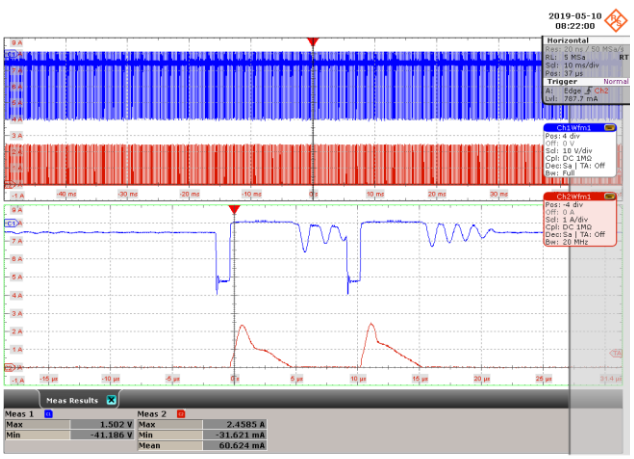

Figure 60 – 230 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 41.19 V.

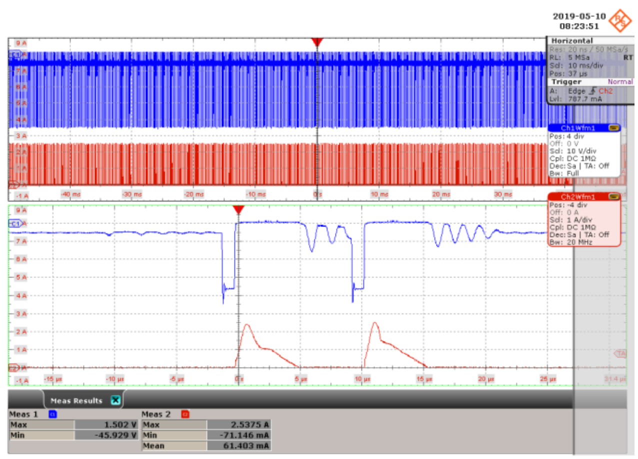

Figure 61 – 265 VAC 60 Hz, Minimum Load.
CH1: V_{FWL_Diode} - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 45.93 V.

14.3.4 Output Diode Voltage and Current at Start-up Operation

14.3.4.1 100% Load

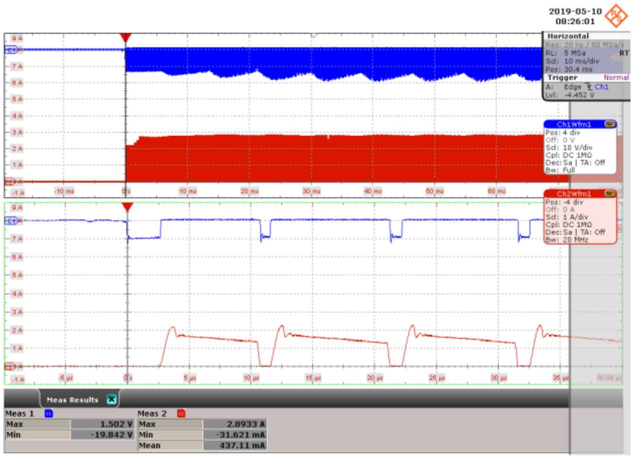

Figure 62 – 85 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 μs / div.
PIV_{MAX} = 19.84 V.

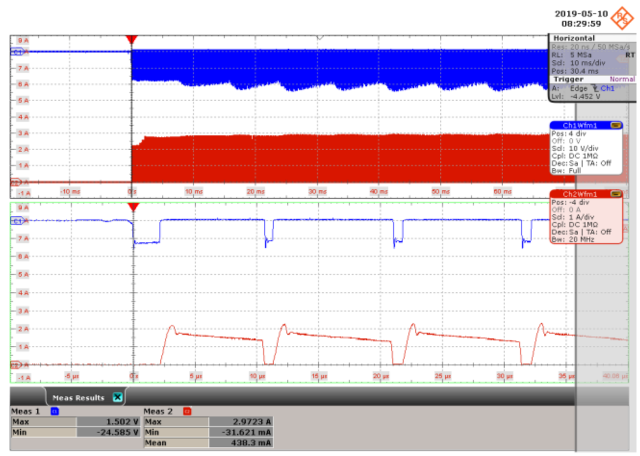

Figure 63 – 115 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 μs / div..
PIV_{MAX} = 24.58 V.

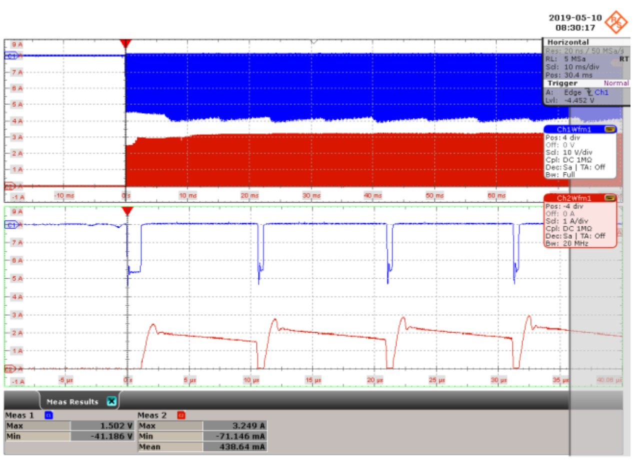

Figure 64 – 230 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 μs / div.
PIV_{MAX} = 41.19 V .

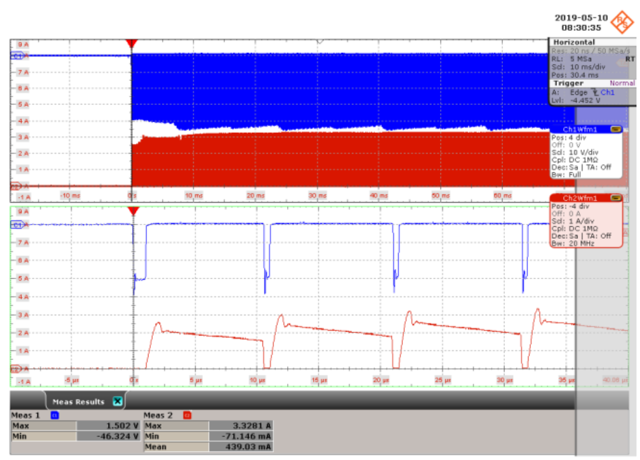

Figure 65 – 265 VAC 60 Hz, Full Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 μs / div..
PIV_{MAX} = 46.32 V.

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14.3.4.2 10% Load

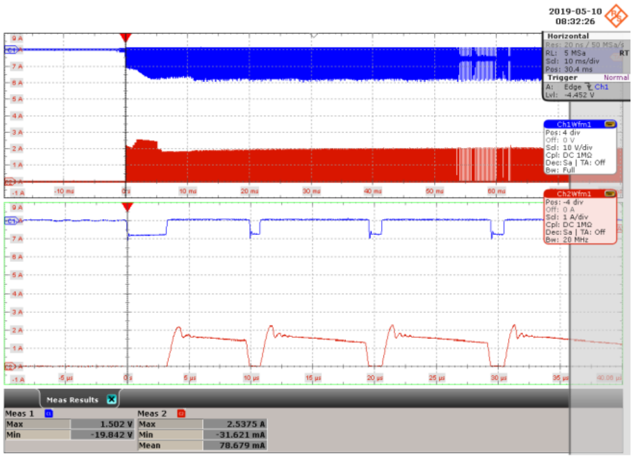

Figure 66 – 85 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 19.84 V.

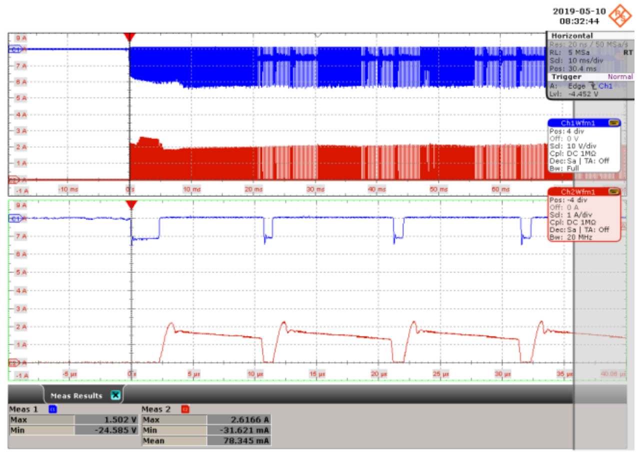

Figure 67 – 115 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 24.59 V.

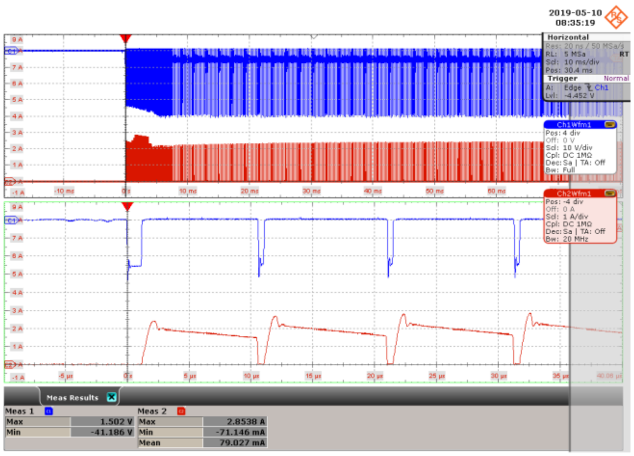

Figure 68 – 230 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 41.19 V.

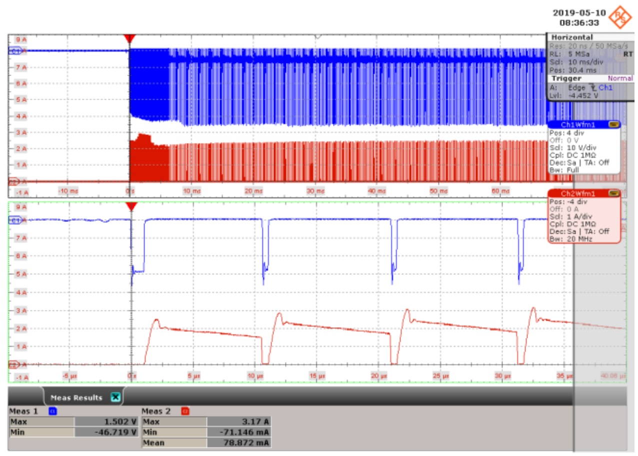

Figure 69 – 265 VAC 60 Hz, Minimum Load.
CH1: $V_{FWL(DIODE)}$ - 10 V / div., 10 ms / div.
CH2: I_{AVE}, 1 A / div., 10 ms / div.
Zoom: 5 µs / div.
PIV_{MAX} = 46.72 V.

14.4 ***Brown-In / Brown-Out Test***

No abnormal overheating nor voltage overshoot / undershoot was observed during and after 0.1 V / s brown-in and brown-out test.

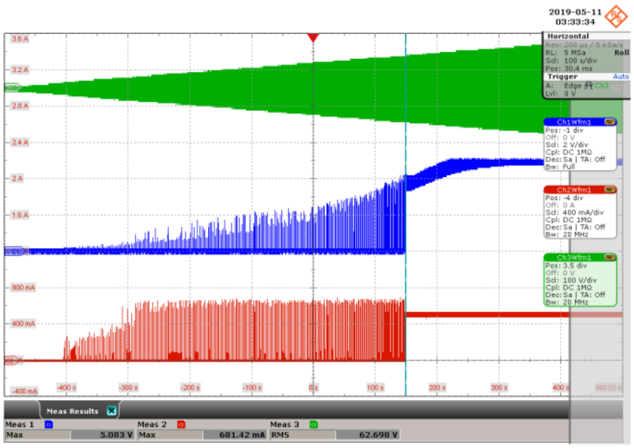

Figure 70 – Brown-in Test.
0 to 85 VAC 0.1 V / s.
CH1: V_{OUT}, 2 V / div., 100 s /div.
CH2: I_{OUT}, 400 mA / div., 100 s / div.
CH3: AC_{IN}, 100 V / div., 100 s / div.

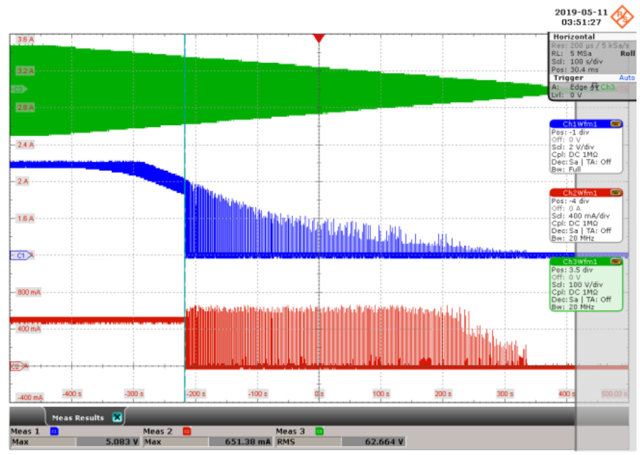

Figure 71 – Brown-out Test.
85 to 0 VAC at 0.1 V / s.
CH1: V_{OUT}, 2 V / div., 100 s /div.
CH2: I_{OUT}, 400 mA / div., 100 s / div.
CH3: AC_{IN}, 100 V / div., 100 s / div.

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14.5 *Output Short-Circuit Auto-restart Test*

Output is shorted at the end of the cable.

Figure 72 – 90 VAC, Normal Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{DS}, 400 V / div., 1 s / div.
$t_{AR(ON)}$: 190 ms.
$t_{AR(OFF)}$: 1.17 s.

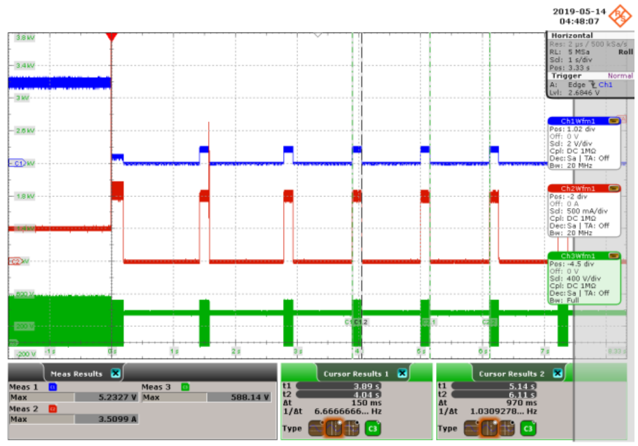

Figure 73 – 265 VAC, Normal Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{DS}, 400 V / div., 1 s / div.
$t_{AR(ON)}$: 150 ms.
$t_{AR(OFF)}$: 0.97 s.

Figure 74 – 90 VAC, Start-up Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{DS}, 400 V / div., 1 s / div.
$t_{AR(ON)}$: 170 ms
$t_{AR(OFF)}$: 1.22 s

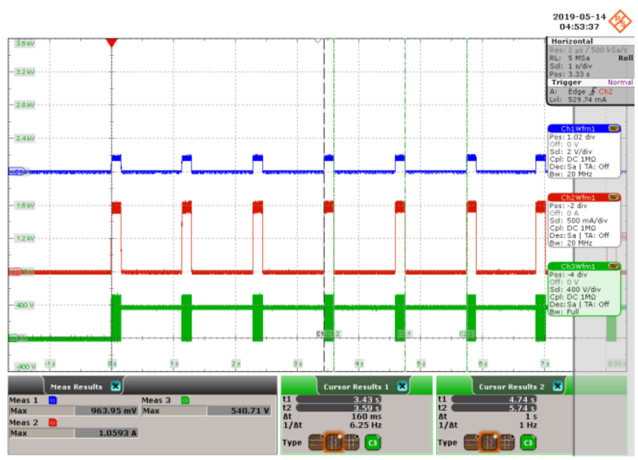

Figure 75 – 265 VAC, Start-up Operation.
CH1: V_{OUT}, 2 V / div., 1 s /div.
CH2: I_{OUT}, 500 mA / div., 1 s / div.
CH3: V_{DS}, 400 V / div., 1 s / div.
$t_{AR(ON)}$: 160 ms
$t_{AR(OFF)}$: 1 s

14.6 ***Output Ripple Measurements***

14.6.1 Output Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1 μF/50 V ceramic type and one (1) 47 μF/50 V aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).

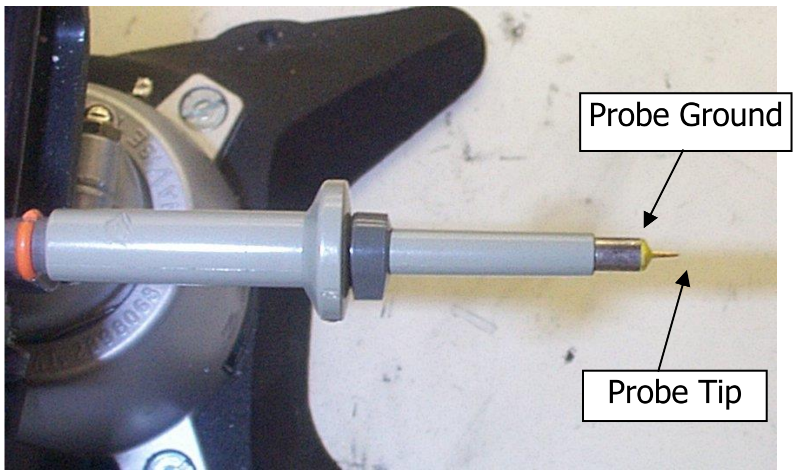

Figure 76 – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

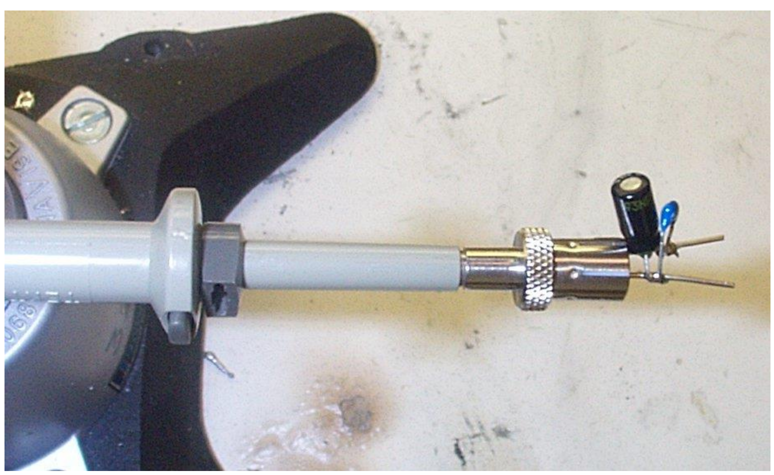

Figure 77 – Oscilloscope Probe with Probe Master (**www.probemaster.com**) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

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14.6.2 Measurement Results

Measured across the PCB connector.

14.6.2.1 100% Load Condition

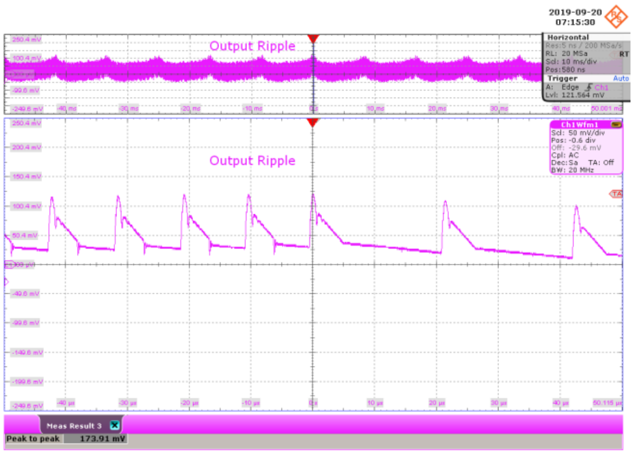

Figure 78 – 85 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 173.91 mV).

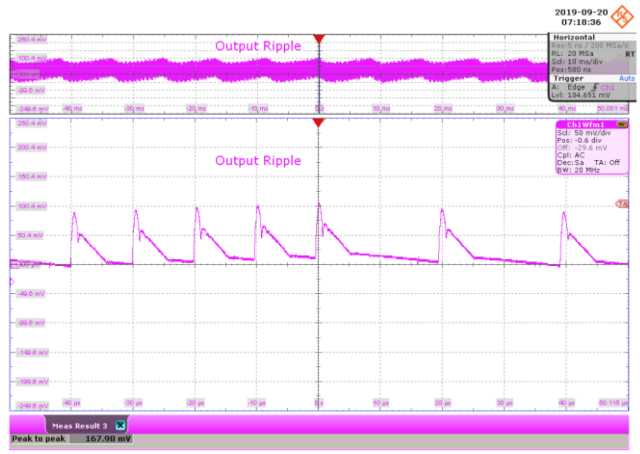

Figure 79 – 115 VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 167.98mV).

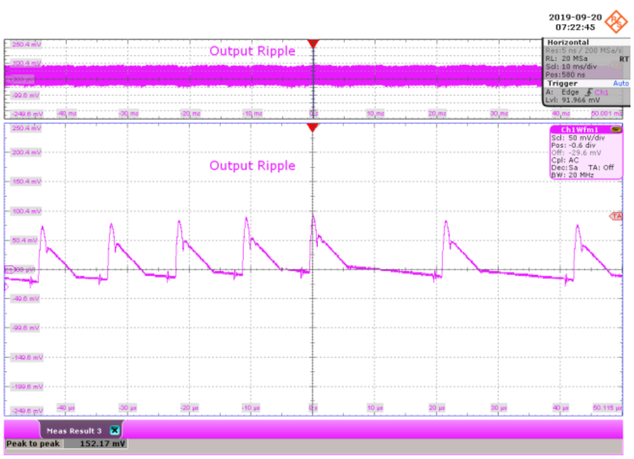

Figure 80 – 230VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 152.17 mV).

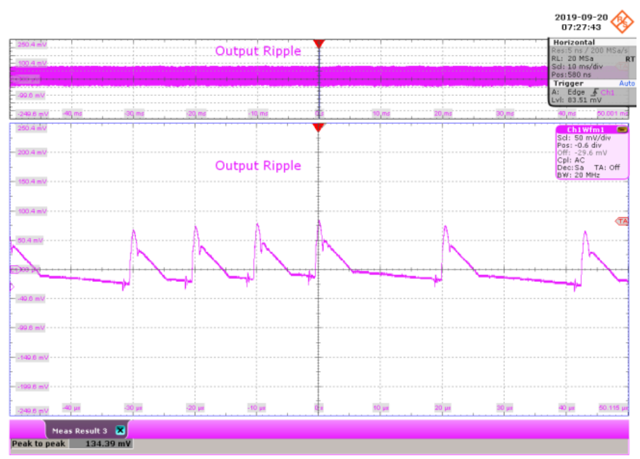

Figure 81 – 265VAC 60 Hz, 100% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 134.39 mV).

14.6.2.2 75% Load Condition

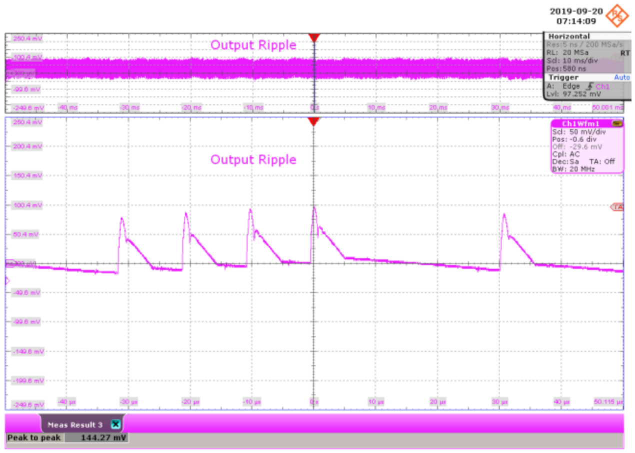

Figure 82 – 85 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 μs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 144.27 mV).

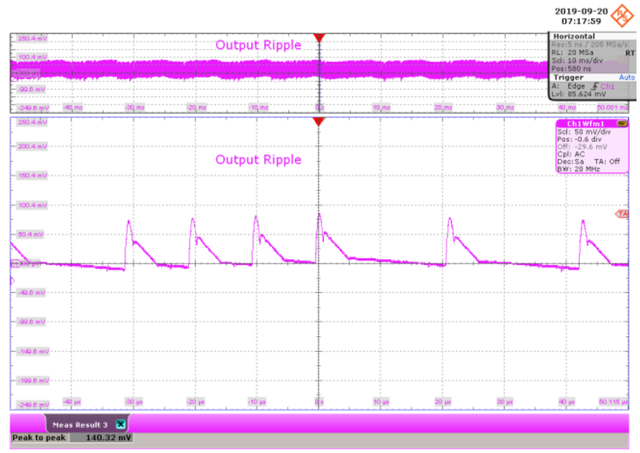

Figure 83 – 115 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 μs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 140.32 mV).

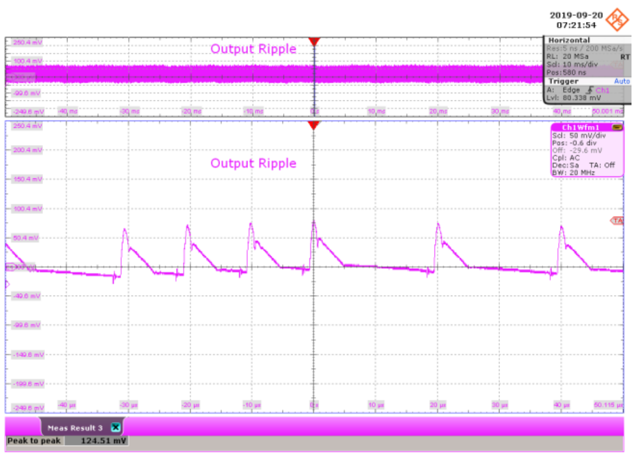

Figure 84 – 230 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 μs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 124.51 mV).

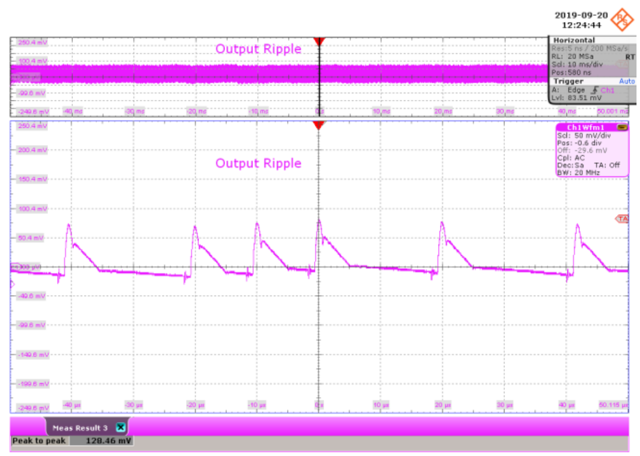

Figure 85 – 265 VAC 60 Hz, 75% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 μs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 128.46 mV).

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14.6.2.3 50% Load Condition

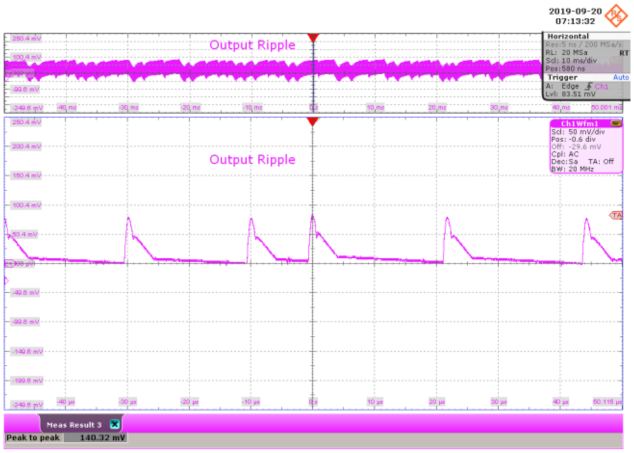

Figure 86 – 85 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 140.32 mV).

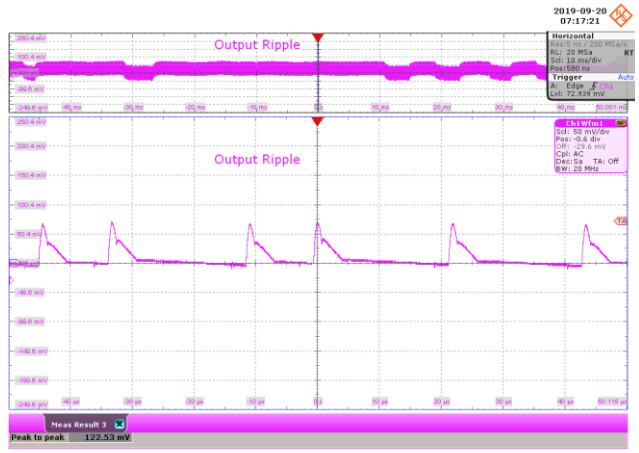

Figure 87 – 115 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 122.53 mV).

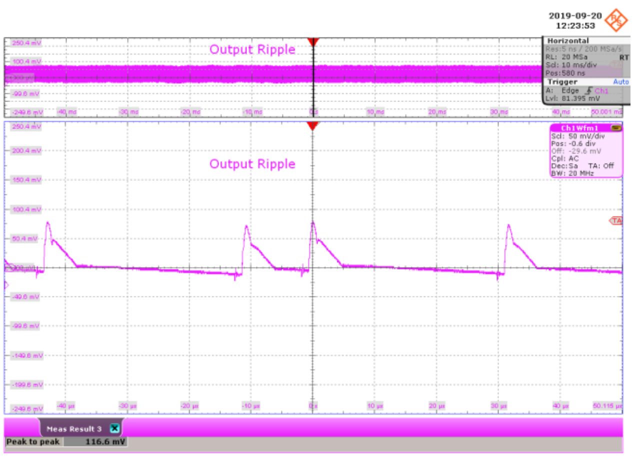

Figure 88 – 230 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 116.6 mV).

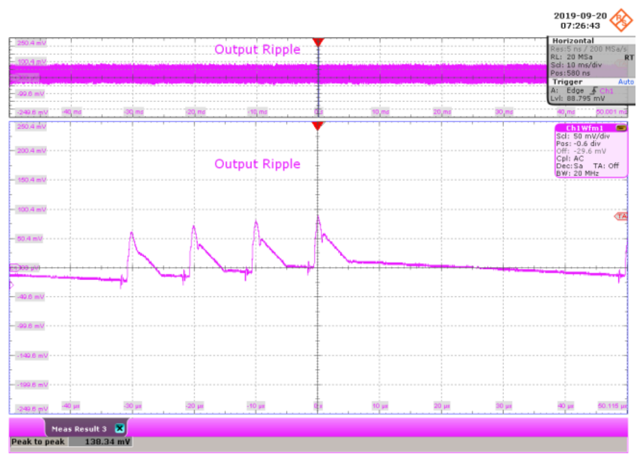

Figure 89 – 265 VAC 60 Hz, 50% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 138.34 mV).

14.6.2.4 25% Load Condition

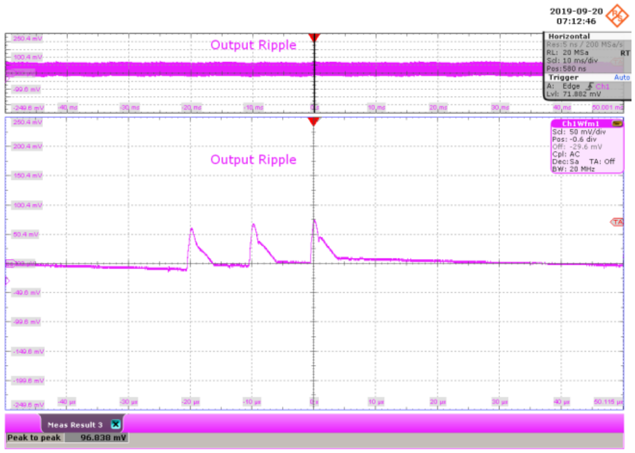

Figure 90 – 85 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 96.838 mV).

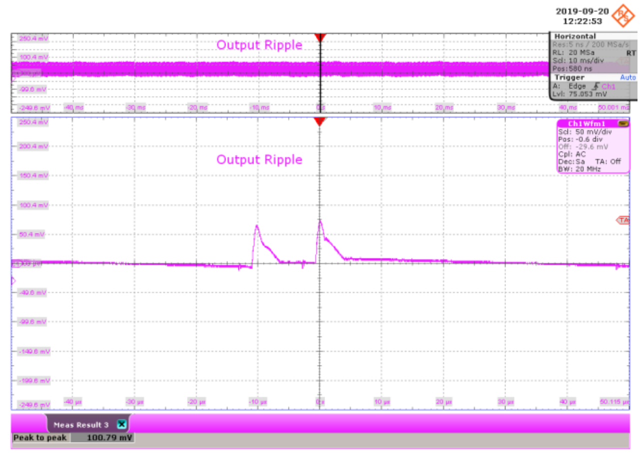

Figure 91 – 115 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ =100.79 mV).

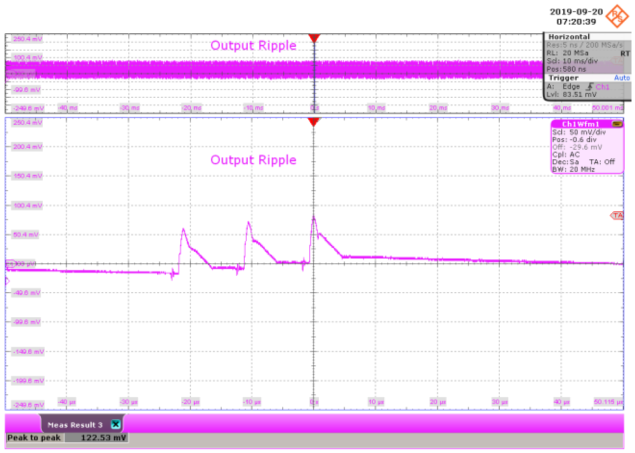

Figure 92 – 230 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 122.53 mV).

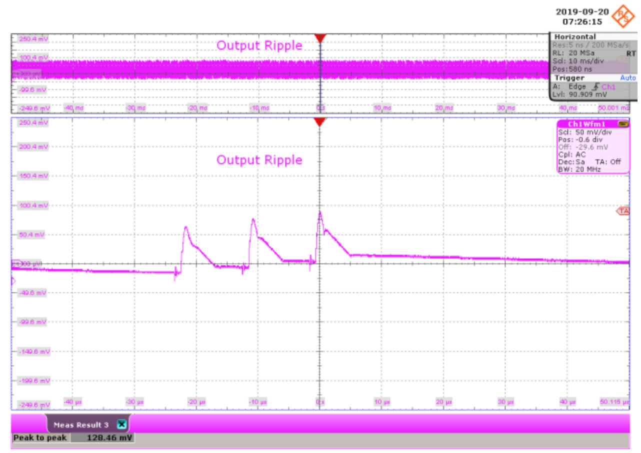

Figure 93 – 265 VAC 60 Hz, 25% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 128.46 mV).

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14.6.2.5 10% Load Condition

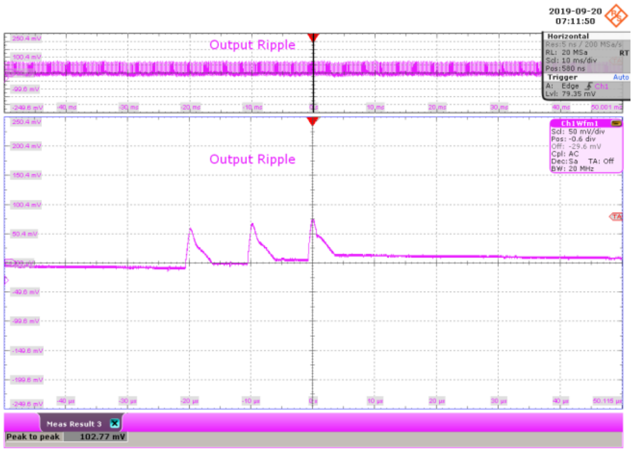

Figure 94 – 85 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 102.77 mV).

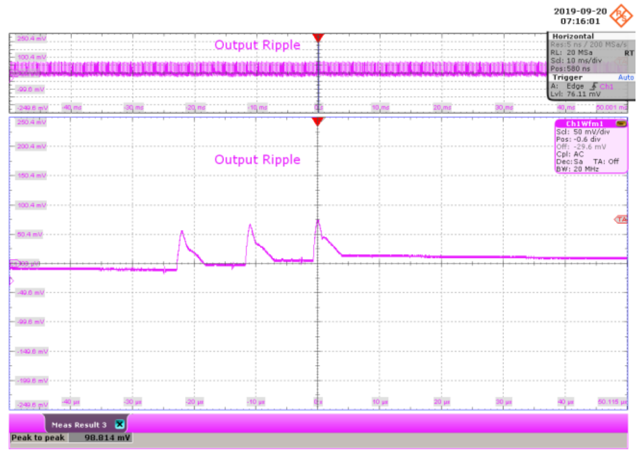

Figure 95 – 115 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 98.814 mV).

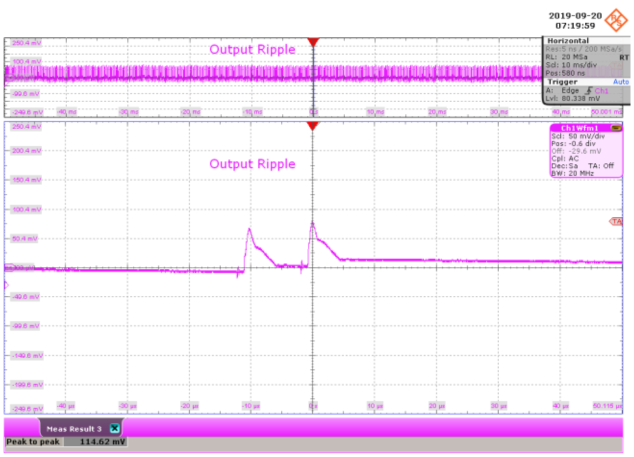

Figure 96 – 230 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 114.62 mV).

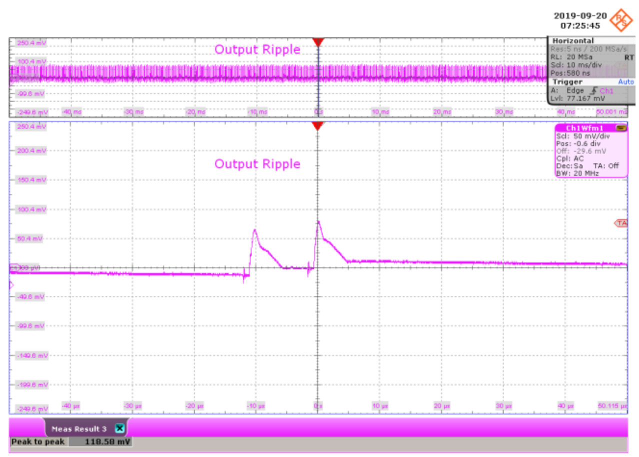

Figure 97 – 265 VAC 60 Hz, 10% Load.
CH1: V_{OUT}, 50 mV / div., 10 ms / div.
Zoom: 10 µs / div.
Voltage Ripple ($V_{OUT(PK-PK)}$ = 118.58 mV).

14.6.3 Output Ripple at Room Temperature

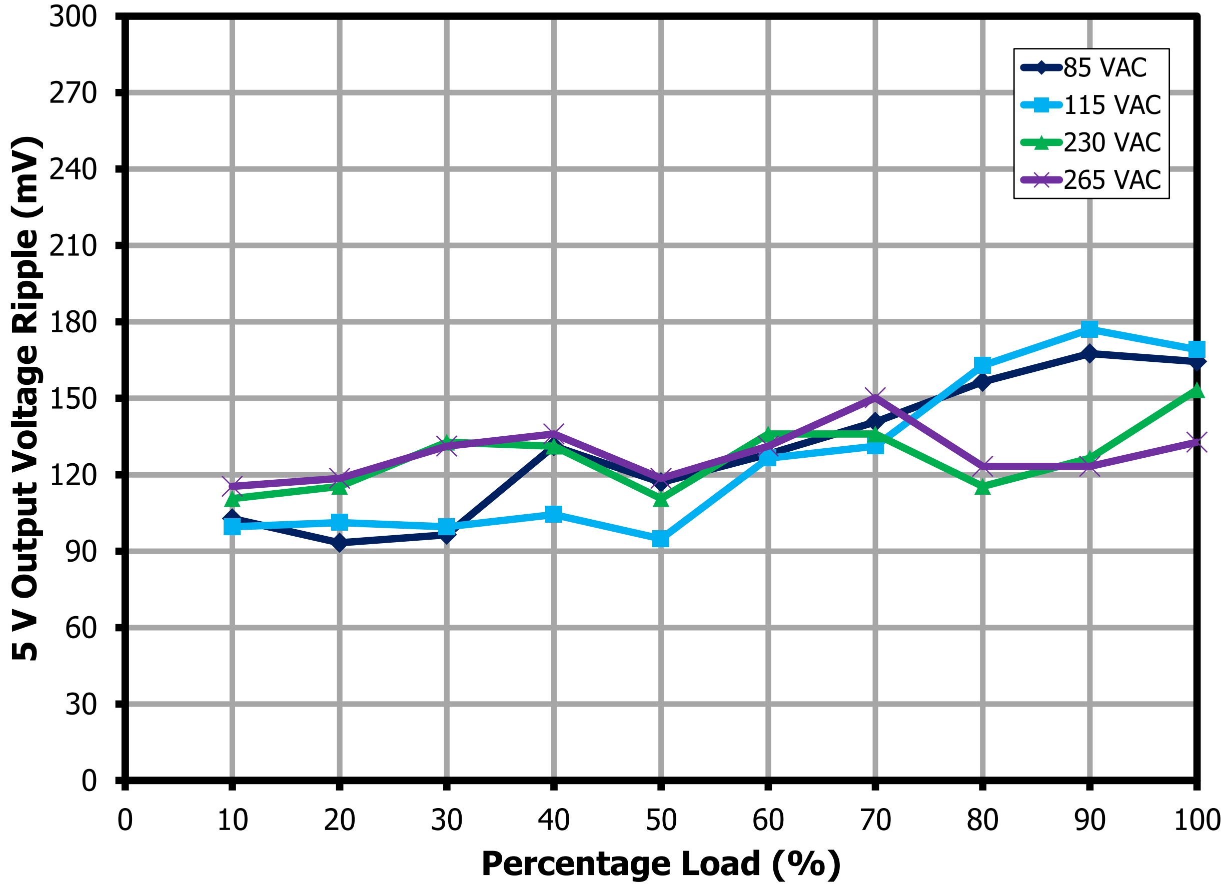

Figure 98 – Output Ripple at Room Temperature.

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15 Conducted EMI

15.1 *Test Set-up*

15.1.1 Equipment and Load Used

1. Rohde and Schwarz ENV216 two line V-network.
2. Rohde and Schwarz ESRP EMI test receiver.
3. Hioki 3322 power hitester.
4. Chroma measurement test fixture.
5. Full Load with input voltage set at 230 VAC and 115 VAC.

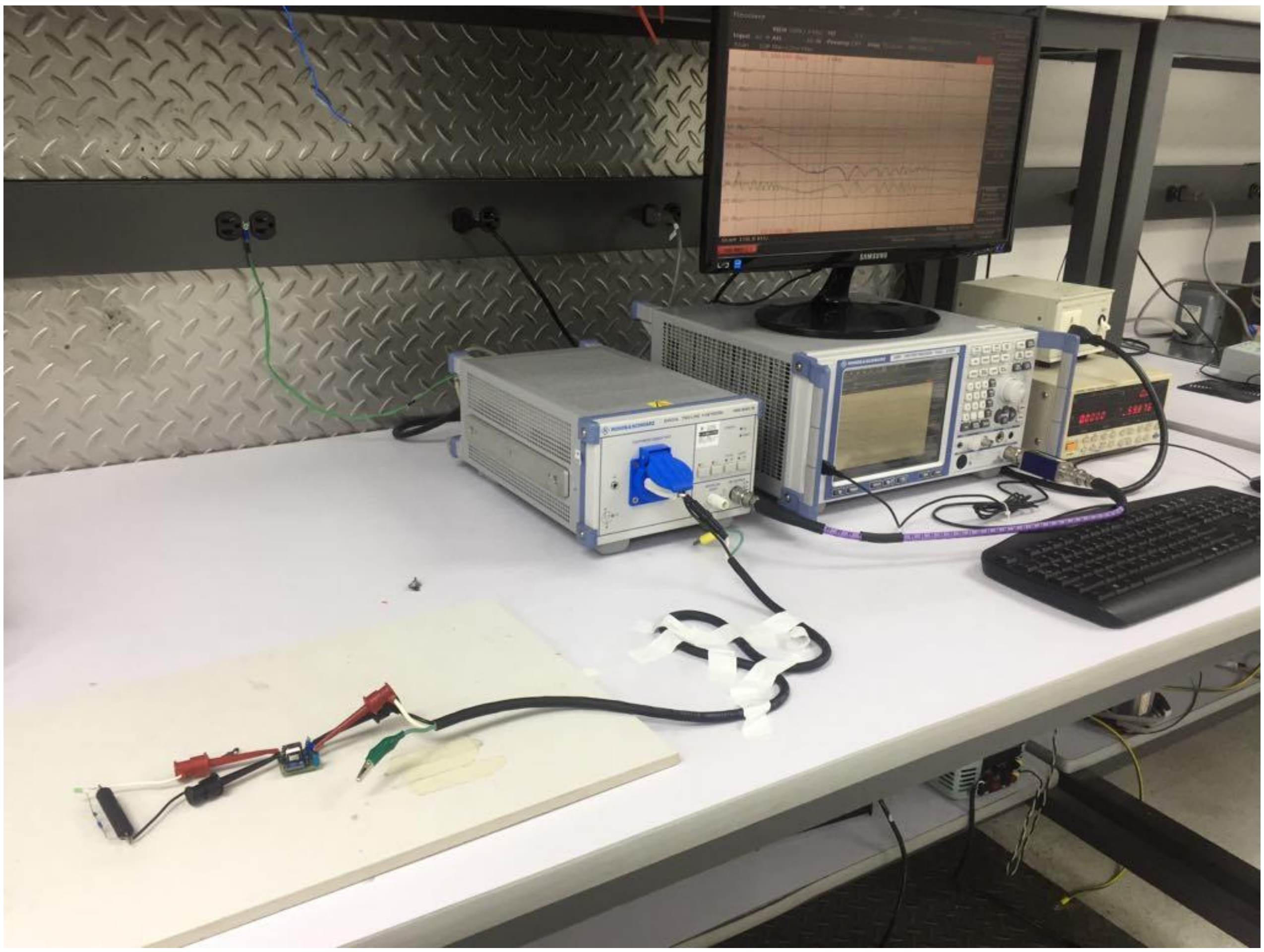
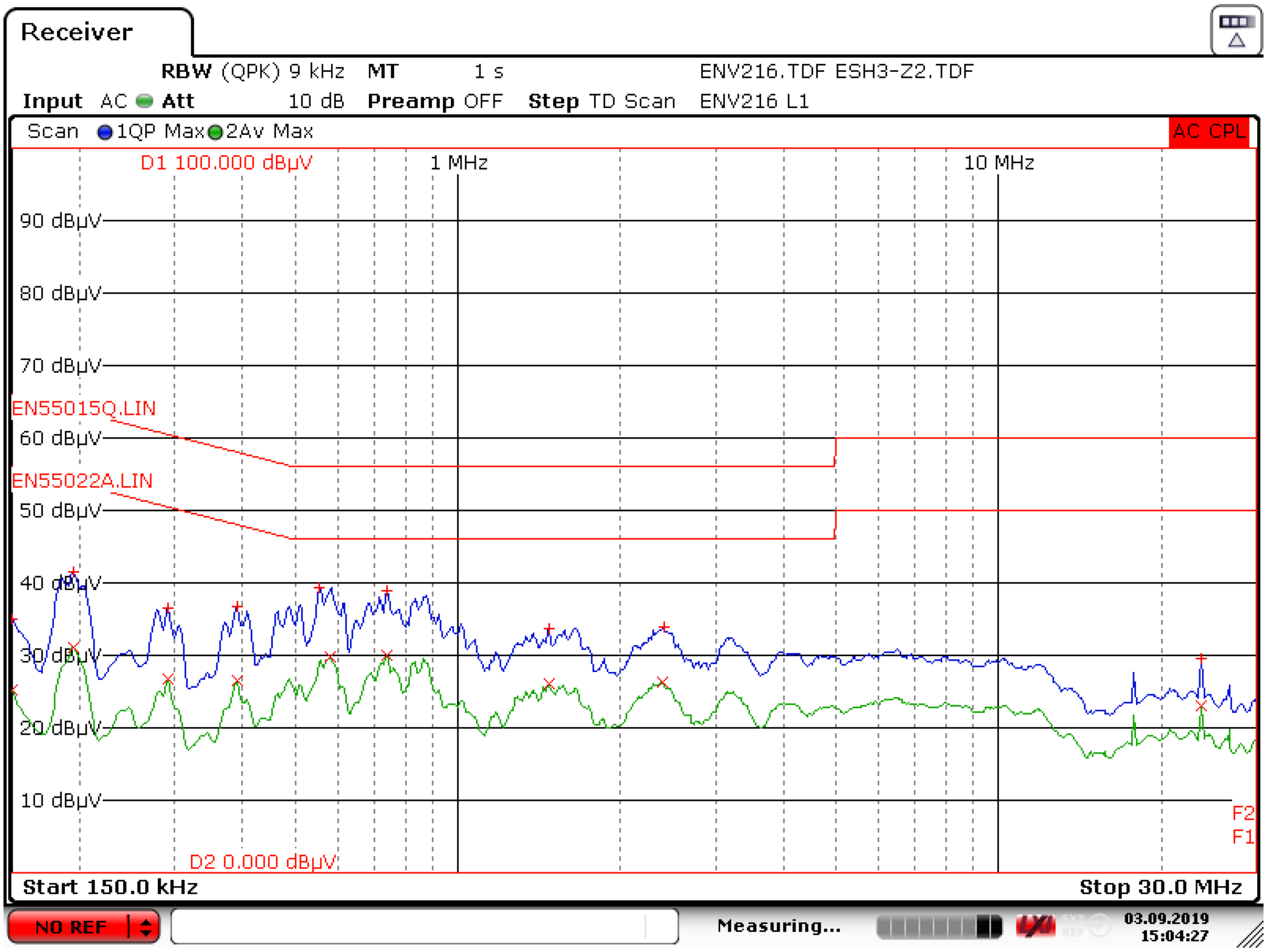


Figure 99 – Conducted EMI Test Set-up.

15.2 *2.5 W Resistive Load, Floating Output*

15.2.1 115 VAC



Date: 3.SEP.2019 15:04:27

Figure 100 – Floating Ground EMI at 115 VAC, Line.

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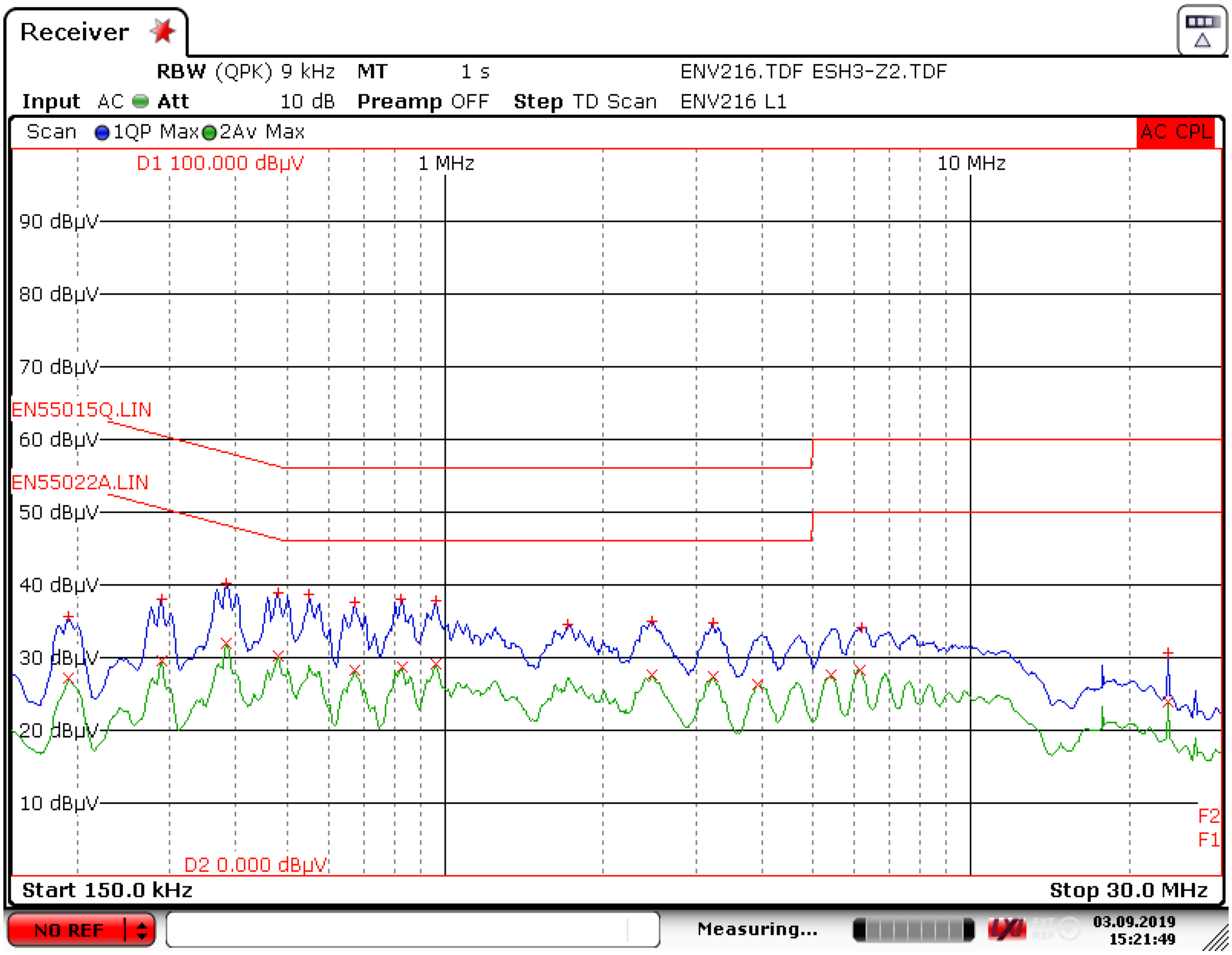
15.2.2 230 VAC



Date: 3.SEP.2019 15:21:49

Figure 101 – Floating Ground EMI at 230 VAC, Line.

16 Line Surge

The unit was subjected to ±1000 V differential surge test using 10 strikes at each condition. A test failure is defined as a non-recoverable interruption of output requiring repair or recycling of input voltage.

16.1 *Differential Surge Test*

Surge Voltage (kV)	Phase Angle (º)	IEC Coupling	Generator Impedance (Ω)	Number Strikes	Result
+1	0	L1 / L2	2	10	PASS
-1	0	L1 / L2	2	10	PASS
+1	90	L1 / L2	2	10	PASS
-1	90	L1 / L2	2	10	PASS
+1	180	L1 / L2	2	10	PASS
-1	180	L1 / L2	2	10	PASS
+1	270	L1 / L2	2	10	PASS
-1	270	L1 / L2	2	10	PASS

Note: In all PASSED results, no damage and no auto-restart were observed.

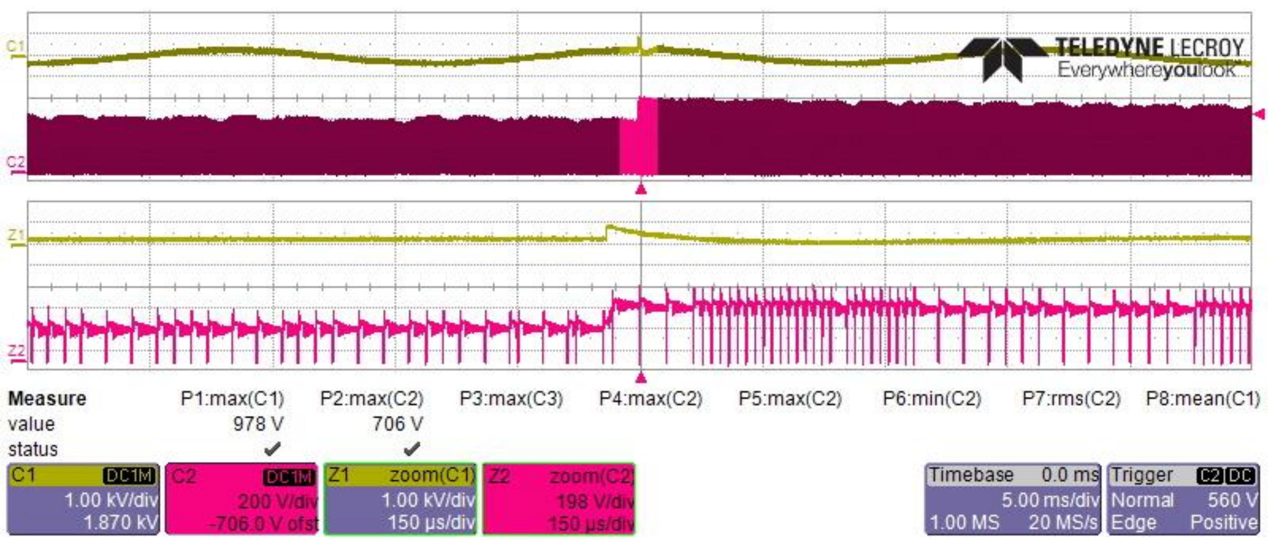


Figure 102 – Input AC Voltage vs. U1 MOSFET V_{DS} during 1 kV Differential Surge.

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17 Audible Noise

17.1 *Audible Noise Smart Plug Test Set-up*

The Smart Plug unit under test was placed inside an acoustic chamber and the microphone was positioned 5 centimeters above the Smart Plug.

Test audible noise using aftermarket Smart Plug. Smart Plug was reworked to change the power supply to DER-831.Test audible noise of uncased Smart Plug and uncased Smart Plug with DER-831.

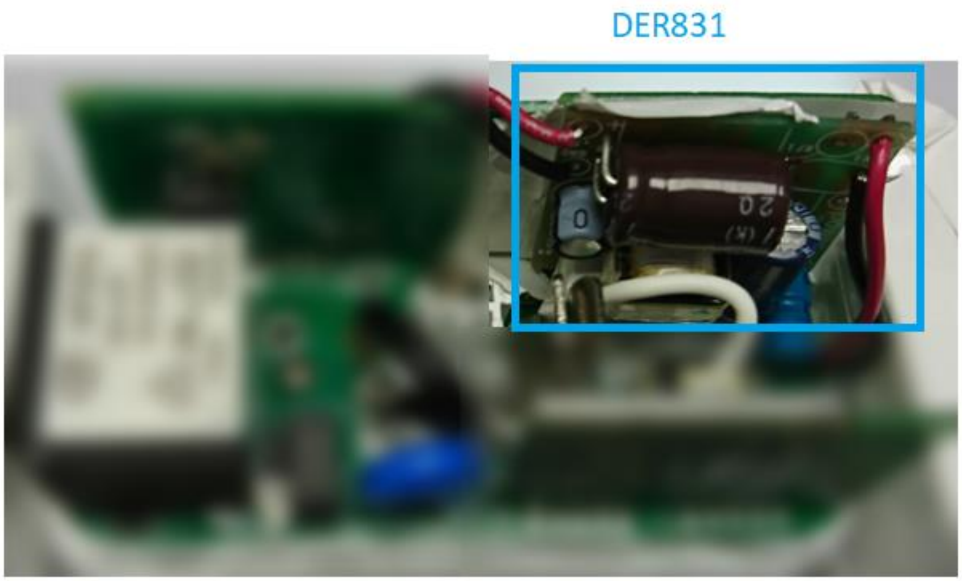

Figure 103 – Reworked After Market Smart Plug with DER-831 Inside

17.2 *Audible Noise Measurements*

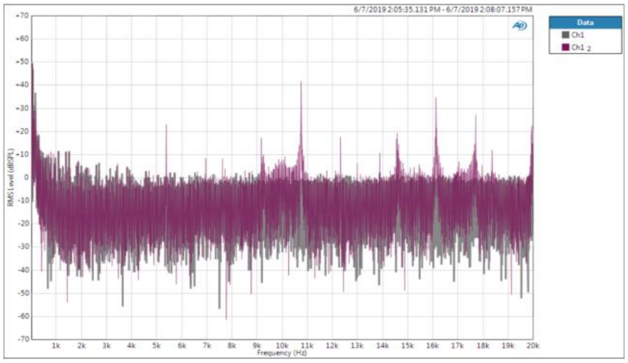

Figure 104 – Uncased Smart Plug.
100 VAC 60 Hz, Smart Plug Disable.

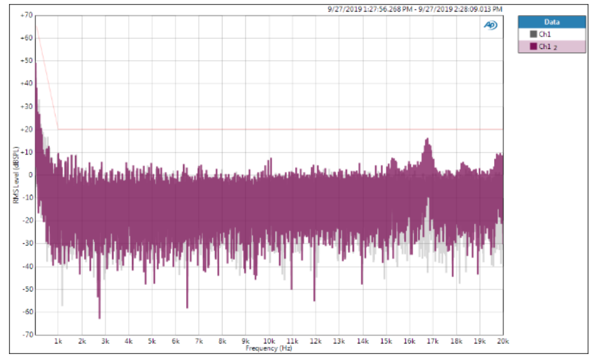

Figure 105 – Uncased Smart Plug with DER-831.
100 VAC 60 Hz, Smart Plug Disable.

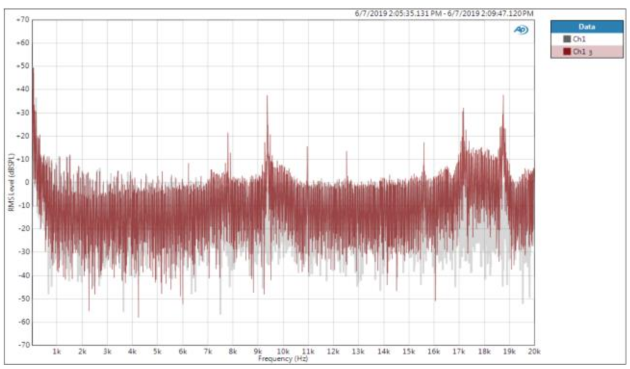

Figure 106 – Uncased Smart Plug.
100 VAC 60 Hz, Smart Plug Enable.

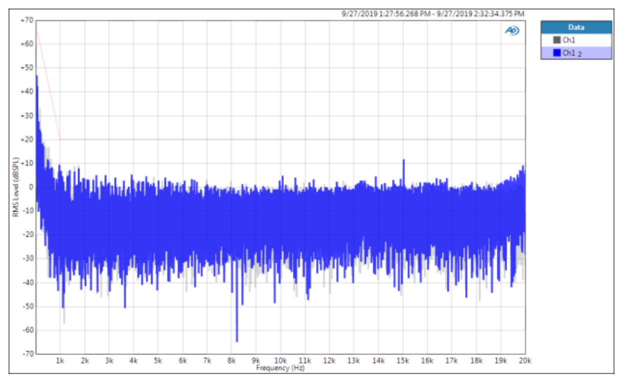

Figure 107 – Uncased Smart Plug with DER-831.
100 VAC 60 Hz, Smart Plug Enable.

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18 Revision History

Date	Author	Revision	Description & Changes	Reviewed
08-Oct-19	CE / RPA	1.0	Initial Release	Apps & Mktg

For the latest updates, visit our website: www.power.com

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