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## Design Example Report

<b>Title</b>	<i>72 W Isolated Flyback Power Supply Using InnoSwitch™ 3-CP PowiGaN™ INN3279C-H215</i>
<b>Specification</b>	90 VAC – 264 VAC Input; 36 V / 2 A Output
<b>Application</b>	Adapter/Charger
<b>Author</b>	Applications Engineering Department
<b>Document Number</b>	DER-903
<b>Date</b>	April 5, 2021
<b>Revision</b>	5.1

### **Summary and Features**

- InnoSwitch3-CP is industry first AC/DC IC with isolated, safety rated integrated feedback
- All the benefits of secondary-side control with the simplicity of primary-side regulation
  - Insensitive to transformer variation
  - Built-in synchronous rectification for high efficiency
- <60 mW no-load input power, 230 VAC
- Primary sensed overvoltage protection
- Very high power density
- Very low component count
- Very high efficiency
  - >92% at 115 VAC and >93% at 230 VAC

### PATENT INFORMATION

The products and applications illustrated herein (including transformer construction and circuits external to the products) may be covered by one or more U.S. and foreign patents, or potentially by pending U.S. and foreign patent applications assigned to Power Integrations. A complete list of Power Integrations' patents may be found at [www.power.com](http://www.power.com). Power Integrations grants its customers a license under certain patent rights as set forth at <https://www.power.com/company/intellectual-property-licensing/>.

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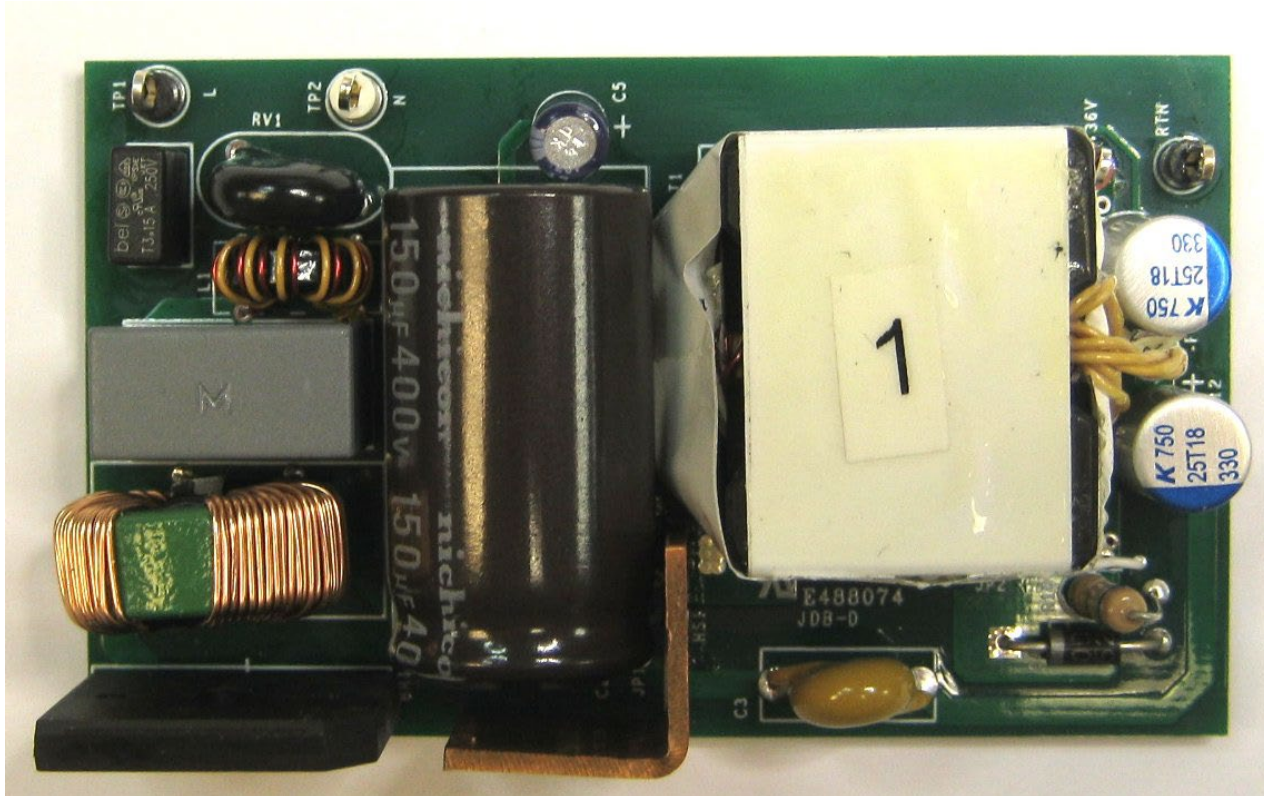
**Important Note:**

Although this board is designed to satisfy safety isolation requirements, the engineering prototype has not been agency approved. Therefore, all testing should be performed using an isolation transformer to provide the AC input to the prototype board.

## 1 Introduction

This document is an engineering report describing a universal input 36 V / 2 A output power supply/charger using the InnoSwitch3-CP INN3279C-H215 flyback controller. This design shows the high power density and efficiency that is possible due to the high level of integration of the InnoSwitch3-CP controller, providing exceptional performance.

This document contains the power supply specification, schematic, bill of materials, transformer documentation, printed circuit layout, and performance data.



**Figure 1** – Populated Circuit Board Photograph, Top.

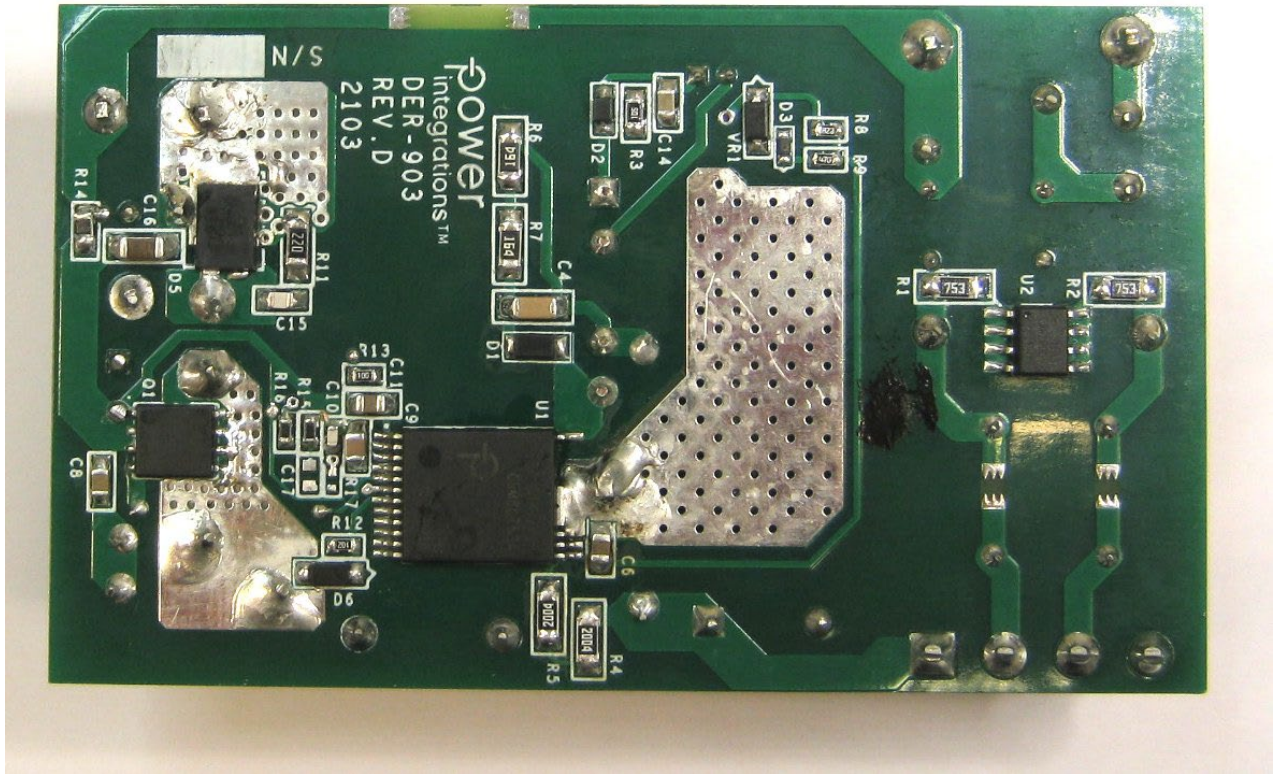


Figure 2 – Populated Circuit Board Photograph, Bottom.

## 2 Power Supply Specification

The table below represents the minimum acceptable performance of the design. Actual performance is listed in the results section.

Description	Symbol	Min	Typ	Max	Units	Comment
<b>Input</b>						
Voltage	<b>V<sub>IN</sub></b>	90		264	VAC	2 Wire – no P.E.
Frequency	<b>f<sub>LINE</sub></b>	47	50/60	64	Hz	
No-load Input Power (230 VAC)				60	mW	Measured at 230 VAC.
<b>Output</b>						
Output Voltage	<b>V<sub>OUT</sub></b>	7	36		V	36V Nominal Output.
Output Ripple Voltage	<b>V<sub>RIPPLE</sub></b>		1		V	p-p On Board.
Output Current	<b>I<sub>OUT</sub></b>	0		2	A	On Board.
Continuous Output Power	<b>P<sub>OUT</sub></b>	0	72		W	
<b>Conducted EMI</b>		Meets CISPR22B / EN55022B				
Safety		Designed to meet IEC60950 / UL1950 Class II				
Ambient Temperature	<b>T<sub>AMB</sub></b>	0		40	°C	Enclosed in Adapter, Sea Level.

### 3 Schematic

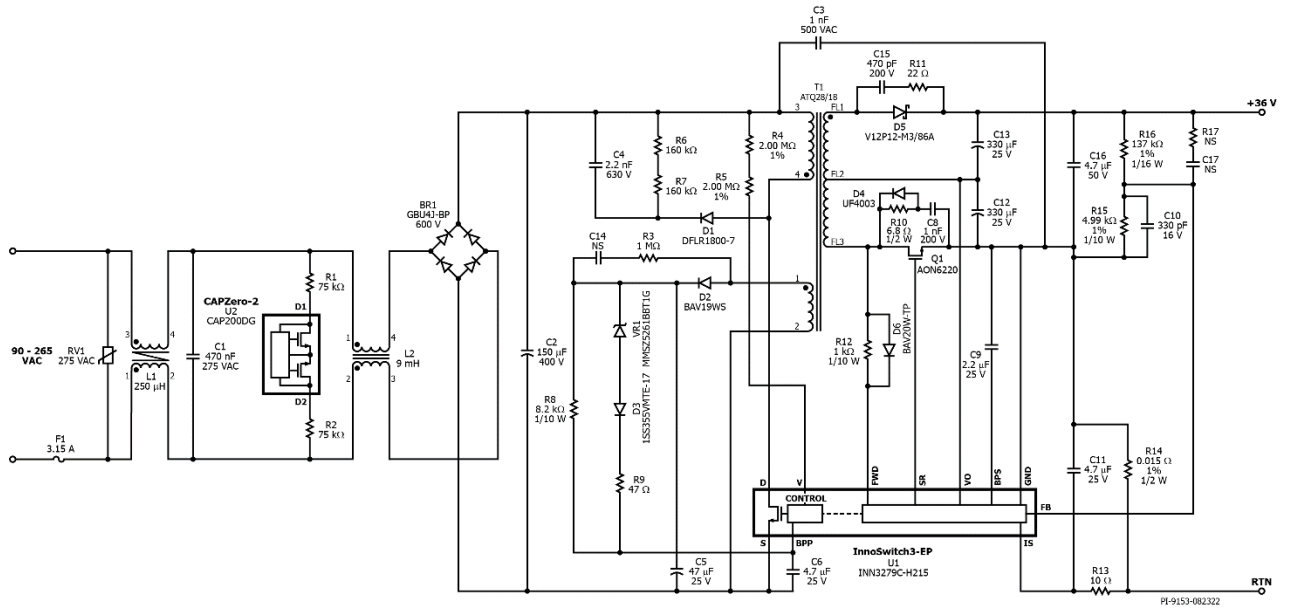


Figure 3 – Schematic.



## 4 Circuit Description

### 4.1 Input EMI Filtering

Fuse F1 isolates the circuit and provides protection from component failure. The common mode chokes L1 and L2 along with capacitors C1 and C3 attenuate EMI. Bridge rectifier BR1 and capacitor C2 rectify the AC line voltage and provide a full wave rectified B+.

Resistors R1 and R2, with U2, discharge capacitor C1 when the power supply is disconnected from AC mains.

Metal oxide varistor (MOV) RV1 protects the circuit during line surge events by effectively clamping the input voltage seen by the power supply.

### 4.2 InnoSwitch3-CP IC Primary

One end of the transformer (T1) primary is connected to the rectified DC bus; the other is connected to the drain terminal of the switch inside the InnoSwitch3-CP IC (U1). Resistors R4-5 provide input voltage sense protection for undervoltage and overvoltage conditions.

An RCD clamp formed by diode D1, resistors R6-7 and capacitor C4 limits the peak drain voltage of U1 at the instant of turn off of the switch inside U1. The clamp helps to dissipate the energy stored in the leakage reactance of transformer T1.

Controller/switch IC U1 is self-starting, using an internal high-voltage current source to charge the BPP pin capacitor (C6) when HVDC is first applied. During normal operation the primary-side block is powered from an auxiliary winding on transformer T1. Output of this auxiliary (or bias) winding is rectified using diode D2 and filtered using capacitor C5. Resistor R8 limits the current being supplied to the BPP pin of the InnoSwitch3-CP IC (U1), while providing enough current to ensure that the high-voltage tap inside U1 is turned off during normal operation. This reduces the low/no-load input power consumption.

Output regulation is achieved using ramp time modulation control, the frequency and  $I_{LIM}$  of switching cycles are adjusted based on the output load. At high load, most switching cycles that are enabled have high value for  $I_{LIM}$  in the selected  $I_{LIM}$  range, and at light load or no-load most cycles are disabled and the ones enabled have low value of  $I_{LIM}$  in the selected  $I_{LIM}$  range. Once a cycle is enabled, the switch will remain on until the primary current ramps to the device current limit for the specific operating state.

Zener diode VR1 and diode D3, along with R9, offers primary sensed output overvoltage protection. In a flyback converter, output of the auxiliary winding tracks the output voltage of the converter. In case of overvoltage at output of the converter, the auxiliary winding voltage increases and causes breakdown of VR1, which then causes a current to flow into the BPP pin of InnoSwitch3-CP IC U1. If the current flowing into the BPP pin increases



above the  $I_{SD}$  threshold, the InnoSwitch3-CP controller will latch off and prevent any further increase in output voltage.

### 4.3 InnoSwitch3-CP IC Secondary

The secondary-side of the InnoSwitch3-CP IC provides output voltage, output current sensing and drive to a MOSFET providing synchronous rectification. The transformer secondary is split into two stacked windings to provide an intermediate voltage feeding the U1 VOUT pin that is within the rating for that pin. This measure is necessary because the 36 V design  $V_{OUT}$  exceeds the U1 VOUT pin voltage rating. The top side of the secondary winding stack is rectified by diode D5 and filtered by C13, while the bottom side is rectified by MOSFET Q1 and filtered by capacitor C12. Capacitor C16 serves to filter the summed output of the two stacked windings. High frequency ringing during switching transients that would otherwise create radiated EMI and/or exceed the PIV ratings of Q1 or D5 is reduced via RCD snubber R10, C8, and D4, as well as RC snubber C15 and R11.

The gate of Q1 is turned on by the secondary-side controller inside IC U1, based on the winding voltage sensed via resistor R12 and D6 and fed into the FWD pin of the IC.

In continuous conduction mode of operation, the MOSFET is turned off just prior to the secondary-side commanding a new switching cycle from the primary. In discontinuous mode of operation, the power MOSFET is turned off when the voltage drop across the MOSFET falls below a threshold of approximately 3 mV. Secondary-side control of the primary-side power switch avoids any possibility of cross conduction of the two switches and provides extremely reliable synchronous rectification.

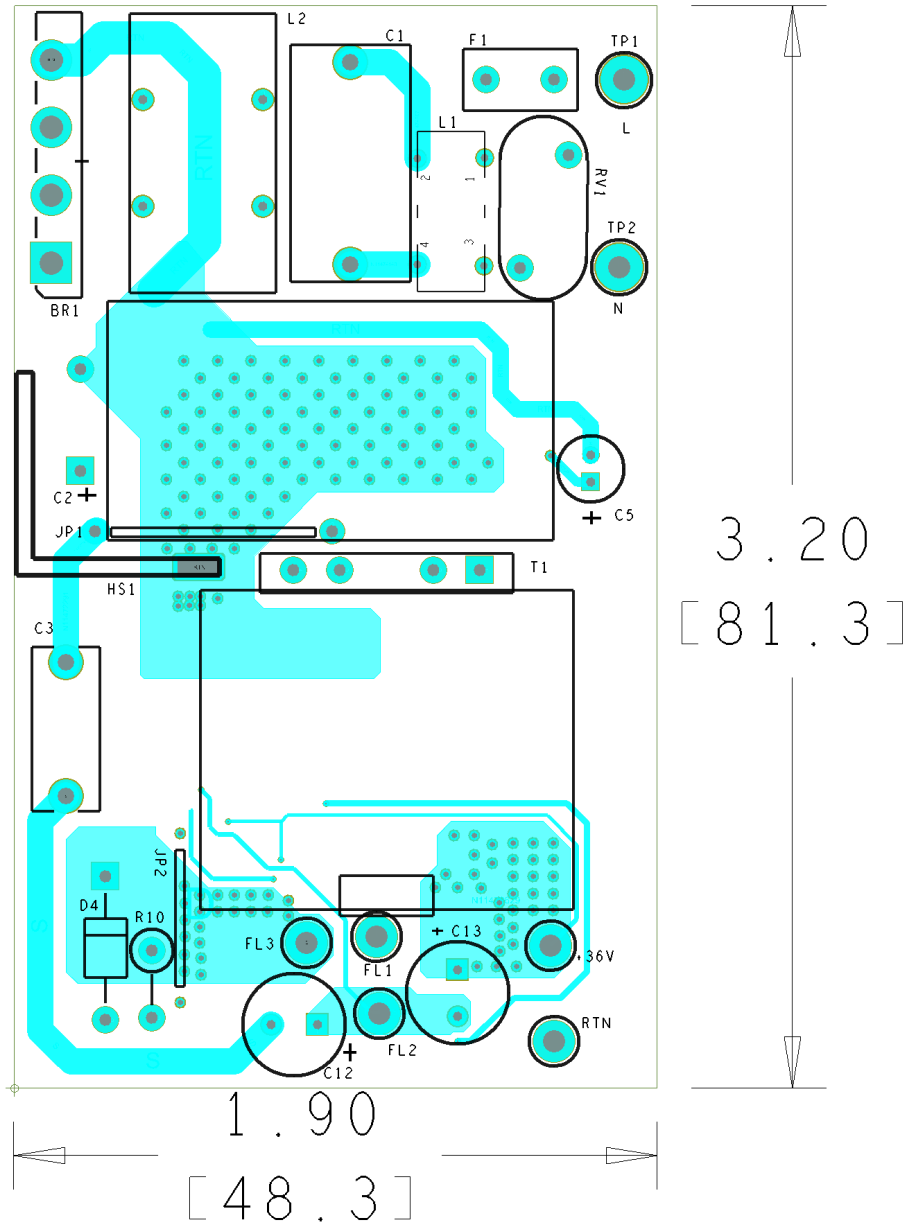
The secondary-side of the IC is self-powered from either the secondary winding forward voltage through R12 and D6 or the intermediate output voltage from the stacked secondary windings. Capacitor C9 connected to the BPS pin of InnoSwitch3-CP IC U1 provides decoupling for the internal circuitry.

Output current is sensed by monitoring the voltage drop across resistor R14 between the IS and GND pins, with a threshold of approximately 35 mV to reduce losses. Resistor R13 and capacitor C11 provide filtering on the IS pin to reduce noise sensitivity.

Output voltage is regulated so as to achieve a voltage of 1.265 V on the FB pin. Resistors R15 – R16 set the nominal output voltage to 36 V. Capacitor C10 provides noise filtering of the signal at the FB pin. Resistor R17 and capacitor C17 (not used in this design) form a phase lead network that ensures stable operation and minimizes output voltage overshoot and undershoot during transient load conditions.

### 5 PCB Layout

PCB copper thickness is 2.0 oz.



**Figure 4 – Printed Circuit Layout, Top.**

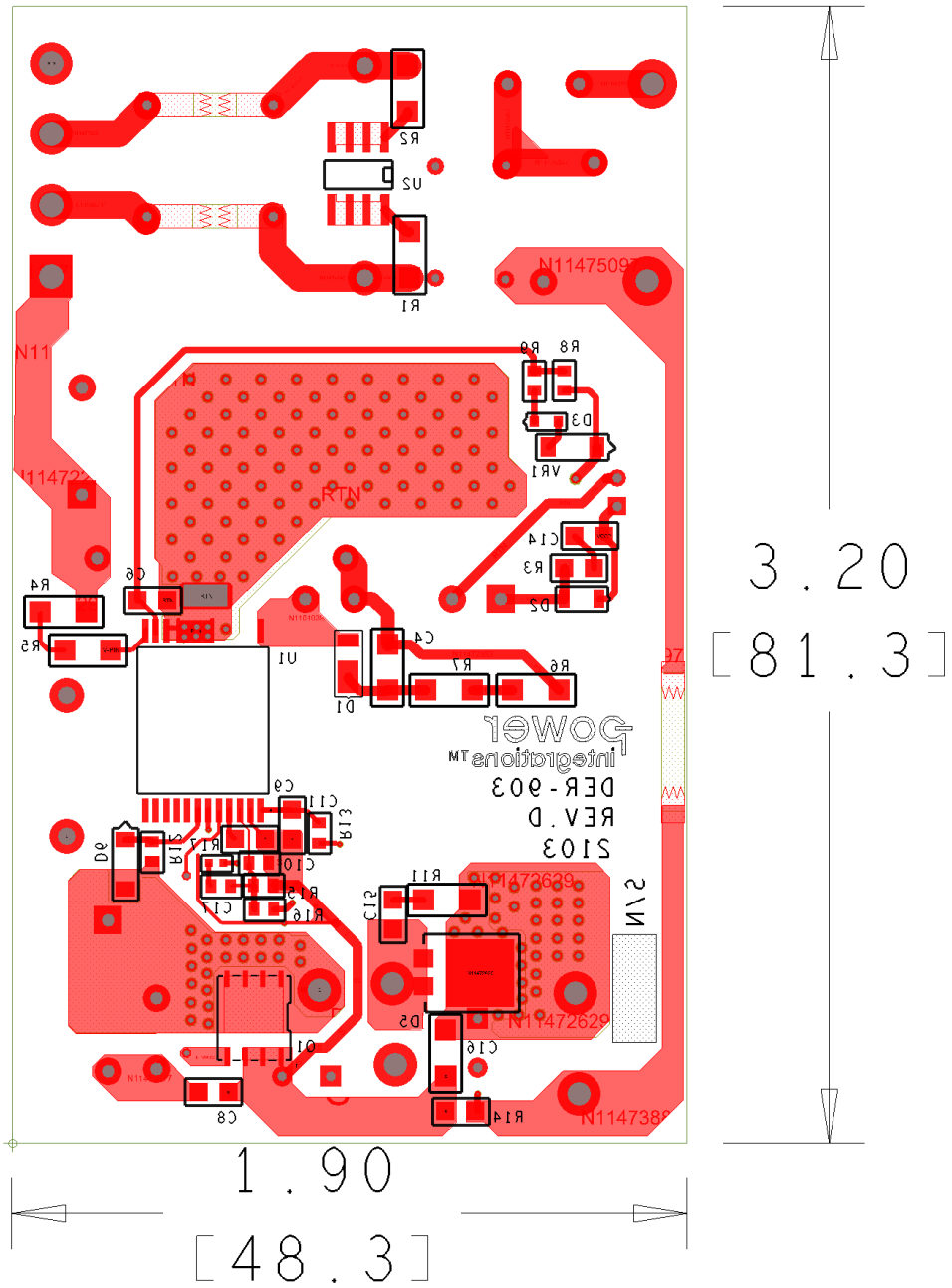


Figure 5 – Printed Circuit Layout, Bottom.



## 6 Bill of Materials

Item	Qty	Part Reference	Description	Mfg Part Number	Mfg
1	1	BR1	600 V, 4 A, Bridge Rectifier, GBU Case	GBU4J-BP	Micro Commercial
2	1	C1	470 nF, 275 VAC, Film, X2	80-R46KI347050P1M	Kemet
3	1	C2	150 $\mu$ F, 20%, ALUM, 400 V, RADIAL, Electrolytic, (18 mm D x 33.5 mm H), Lead spacing 0.295" (7.50 mm)	UCP2G151MHD6	Nichicon
4	1	C3	1 nF, 500 VAC, Ceramic, Y1	VY1102M35Y5UG63V0	Vishay
5	1	C4	2.2 nF, 630 V, Ceramic, X7R, 1206	C3216X7R2J222K115AA	TDK
6	1	C5	47 $\mu$ F, 25 V, Electrolytic, Low ESR, 500 m $\Omega$ , (5 x 11.5)	ELXZ250ELL470MEB5D	Nippon Chemi-Con
7	2	C6 C11	4.7 $\mu$ F $\pm$ 10%, 25V, X7R, 0805, -55°C ~ 125°C	TMK212AB7475KG-T	Taiyo Yuden
8	2	C8 C14	1 nF, 200 V, Ceramic, X7R, 0805	08052C102KAT2A	AVX
9	1	C9	2.2 $\mu$ F, 25 V, Ceramic, X7R, 0805	C2012X7R1E225M125AB	TDK
10	1	C10	330 pF, $\pm$ 5%, 50V, Ceramic, COG, NP0, 0603	C0603C331J5GACAUTO	KEMET
11	2	C12 C13	330 $\mu$ F, $\pm$ 20%, 25 V, Al Organic Polymer, Gen. Purpose, Can, 18 m $\Omega$ , 2000 Hrs @ 105°C, (8 mm x 13 mm)	A750KS337M1EAAE018	KEMET
12	1	C15	470 pF, 200 V, Ceramic, X7R, 0805	C0805C471K2RACTU	Kemet
13	1	C16	4.7 $\mu$ F, 50 V, Ceramic, X7R, 1206	UMK316AB7475KL-T	Taiyo Yuden
14	1	C17	10 nF 50 V, Ceramic, X7R, 0603	C0603C103K5RACTU	Kemet
15	1	D1	800 V, 1 A, Rectifier, POWERDI123	DFLR1800-7	Diodes, Inc.
16	1	D2	100 V, 0.2 A, Fast Switching, 50 ns, SOD-323	BAV19WS-7-F	Diodes, Inc.
17	1	D3	Diode SML SIG 80 V 100 mA SSMINI2	1SS355VMTE-17	Rohm Semi
18	1	D4	200 V, 1 A, Ultrafast Recovery, 50 ns, DO-41	UF4003-E3	Vishay
19	1	D5	Diode, Schottky, 120V, 12A, SMT, TO-277A (SMPC)	V12P12-M3/86A	Vishay
20	1	D6	150 V, 0.2 A, SOD-123	BAV20W-TP	Micro Commercial
21	1	F1	3.15 A, 250 V, Slow, RST	507-1181	Belfuse
22	1	HS1	SHTM, HEAT SINK, DER903	61-00287-00	Power Integrations
23	1	JP1	Wire Jumper, Non-insulated, #22 AWG, 0.7 in	298	Alpha
24	1	JP2	Wire Jumper, Insulated, #28 AWG, 0.5 in	2842/1 WH005	Alpha Wire
25	1	L1	600 $\mu$ H, Toroidal Common Mode Choke, custom, DER-536, wound on 32-00275-00 core, Added FP for DER601 lkn110117.	32-00347-00	Power Integrations
26	1	L2	9 mH, 2 A, Common Mode Choke	T18107V-902S P.I. Custom	Fontaine Technologies
27	1	Q1	MOSFET, N-CH, 100 V, 48 A (Tc), 113.5W (Tc), DFN5X6, 8-DFN (5x6)	AON6220	Alpha & Omega Semi
28	2	R1 R2	RES, 75 k $\Omega$ , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ753V	Panasonic
29	1	R3	RES, 1.0 M $\Omega$ , 5%, 1/8 W, Thick Film, 0805	ERJ-6GEYJ105V	Panasonic
30	2	R4 R5	RES, 2.00 M $\Omega$ , 1%, 1/4 W, Thick Film, 1206	ERJ-8ENF2004V	Panasonic
31	2	R6 R7	RES, 160 k $\Omega$ , 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ164V	Panasonic
32	1	R8	RES, 8.2 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ822V	Panasonic
33	1	R9	RES, 47 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ470V	Panasonic
34	1	R10	RES, 6.8 $\Omega$ , 5%, 1/2 W, Carbon Film	CFR-50JB-6R8	Yageo
35	1	R11	RES, 22 R $\Omega$ 5%, 1/4 W, Thick Film, 1206	ERJ-8GEYJ220V	Panasonic
36	1	R12	RES, 1 k $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ102V	Panasonic
37	1	R13	RES, 10 $\Omega$ , 5%, 1/10 W, Thick Film, 0603	ERJ-3GEYJ100V	Panasonic
38	1	R14	RES, 0.015 $\Omega$ , 0.5 W, 1%, 0805	ERJ-6BWFRO15V	Panasonic
39	1	R15	RES, 4.99 k $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF4991V	Panasonic
40	1	R16	RES, 137 k $\Omega$ , 1%, 1/16 W, Thick Film, 0603	ERJ-3EKF1373V	Panasonic



41	1	R17	RES, 6.2 k $\Omega$ , 5%, 1/16 W, Thick Film, 0402	RC0402JR-076K2L	Yageo
42	1	RV1	275 VAC, 80J, 10 mm, RADIAL	ERZ-V10D431	Panasonic
43	1	T1	Transformer, ATQ28/18, Vertical, 4 pins.	Custom	Custom
44	2	TP1 TP4	Test Point, BLK, THRU-HOLE MOUNT	5011	Keystone
45	1	TP2	Test Point, WHT, THRU-HOLE MOUNT	5012	Keystone
46	1	TP3	Test Point, RED, THRU-HOLE MOUNT	5010	Keystone
47	1	U1	InnoSwitch3-CP Switch Integrated Circuit, InSOP24D	INN3279C-H215	Power Integrations
48	1	U2	CAPZero-2, SO-8C	CAP200DG	Power Integrations
49	1	VR1	DIODE ZENER 47 V 500 mW SOD123	MMSZ5261BT1G	ON Semi

## 7 Flyback Transformer Design Spreadsheet

ACDC_InnoSwitch3-CP_Flyback_072619; Rev.1.5; Copyright Power Integrations 2018	INPUT	INFO	OUTPUT	UNITS	InnoSwitch3-CP Flyback Design Spreadsheet
<b>APPLICATION VARIABLES</b>					
VIN_MIN	90		90	V	Minimum AC input voltage
VIN_MAX	264		264	V	Maximum AC input voltage
VIN_RANGE			UNIVERSAL		Range of AC input voltage
LINEFREQ			60	Hz	AC Input voltage frequency
CAP_INPUT	150.0		150.0	uF	Input capacitor
VOUT	36.00	Warning	36.00	V	The output voltage exceeds the VOUT Pin voltage rating. Reduce the output voltage
PERCENT_CDC			0%		Percentage (of output voltage) cable drop compensation desired at full load
IOUT	2.000		2.000	A	Output current
POUT			72.00	W	Output power
EFFICIENCY	0.93		0.93		AC-DC efficiency estimate at full load given that the converter is switching at the valley of the rectified minimum input AC voltage
FACTOR_Z			0.50		Z-factor estimate
ENCLOSURE	ADAPTER		ADAPTER		Power supply enclosure
<b>PRIMARY CONTROLLER SELECTION</b>					
ILIMIT_MODE	INCREASED		INCREASED		Device current limit mode
DEVICE_GENERIC	AUTO		INN3279C		Generic device code
DEVICE_CODE			INN3279C		Actual device code
POUT_MAX			75	W	Power capability of the device based on thermal performance
RDSON_100DEG			0.62	Ω	Primary switch on time drain resistance at 100degC
ILIMIT_MIN			1.980	A	Minimum current limit of the primary switch
ILIMIT_TYP			2.130	A	Typical current limit of the primary switch
ILIMIT_MAX			2.279	A	Maximum current limit of the primary switch
VDRAIN_BREAKDOWN			750	V	Device breakdown voltage
VDRAIN_ON_PRSW			0.48	V	Primary switch on time drain voltage
VDRAIN_OFF_PRSW			563.4	V	Peak drain voltage on the primary switch during turn-off
<b>WORST CASE ELECTRICAL PARAMETERS</b>					
FSWITCHING_MAX	90000		90000	Hz	Maximum switching frequency at full load and valley of the rectified minimum AC input voltage
VOR	120.0		120.0	V	Secondary voltage reflected to the primary when the primary switch turns off
VMIN			97.71	V	Valley of the minimum input AC voltage at full load
KP			0.57		Measure of continuous/discontinuous mode of operation
MODE_OPERATION			CCM		Mode of operation
DUTYCYCLE			0.552		Primary switch duty cycle
TIME_ON			11.32	us	Primary switch on-time
TIME_OFF			4.97	us	Primary switch off-time
LPRIMARY_MIN			524.7	uH	Minimum primary inductance



LPRIMARY_TYP			552.3	uH	Typical primary inductance
LPRIMARY_TOL			5.0	%	Primary inductance tolerance
LPRIMARY_MAX			580.0	uH	Maximum primary inductance
<b>PRIMARY CURRENT</b>					
IPEAK_PRIMARY			2.167	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.838	A	Primary switch current pedestal
I AVG_PRIMARY			0.768	A	Primary switch average current
IRIPPLE_PRIMARY			1.552	A	Primary switch ripple current
IRMS_PRIMARY			1.086	A	Primary switch RMS current
<b>SECONDARY CURRENT</b>					
IPEAK_SECONDARY			7.430	A	Secondary winding peak current
IPEDESTAL_SECONDARY			2.873	A	Secondary winding current pedestal
IRMS_SECONDARY			3.352	A	Secondary winding RMS current
<b>TRANSFORMER CONSTRUCTIONPARAMETERS</b>					
<b>CORE SELECTION</b>					
CORE	CUSTOM		CUSTOM		Core selection
CORE CODE	ATQ28-18		ATQ28-18		Core code
AE	156.00		156.00	mm <sup>2</sup>	Core cross sectional area
LE	47.80		47.80	mm	Core magnetic path length
AL	3000		3000	nH/turns <sup>2</sup>	Ungapped core effective inductance
VE	7456.0		7456.0	mm <sup>3</sup>	Core volume
BOBBIN	1tq28		1tq28		Bobbin
AW	42.80		42.80	mm <sup>2</sup>	Window area of the bobbin
BW	8.50		8.50	mm	Bobbin width
MARGIN			0.0	mm	Safety margin width (Half the primary tosecondary creepage distance)
<b>PRIMARY WINDING</b>					
NPRIMARY			24		Primary turns
BPEAK			3613	Gauss	Peak flux density
BMAX			3320	Gauss	Maximum flux density
BAC			1166	Gauss	AC flux density (0.5 x Peak to Peak)
ALG			959	nH/turns <sup>2</sup>	Typical gapped core effective inductance
LG			0.139	mm	Core gap length
LAYERS_PRIMARY			2		Number of primary layers
AWG_PRIMARY			23	AWG	Primary winding wire AWG
OD_PRIMARY_INSULATED			0.642	mm	Primary winding wire outer diameter withinsulation
OD_PRIMARY_BARE			0.573	mm	Primary winding wire outer diameter withoutinsulation
CMA_PRIMARY			469	Cmil/A	Primary winding wire CMA
<b>SECONDARY WINDING</b>					
NSECONDARY			7		Secondary turns
AWG_SECONDARY			21	AWG	Secondary winding wire AWG
OD_SECONDARY_INSULATED			1.029	mm	Secondary winding wire outer diameter withinsulation
OD_SECONDARY_BARE			0.723	mm	Secondary winding wire outer diameter without insulation
CMA_SECONDARY			242	Cmil/A	Secondary winding wire CMA
<b>BIAS WINDING</b>					



NBIAS			3		Bias turns
<b>PRIMARY COMPONENTS SELECTION</b>					
<b>LINE UNDERVOLTAGE</b>					
BROWN-IN REQUIRED			72.0	V	Required AC RMS line voltage brown-in threshold
RLS			3.64	MΩ	Connect two 1.82 MOhm resistors to the V-pin for the required UV/OV threshold
BROWN-IN ACTUAL			73.0	V	Actual AC RMS brown-in threshold
BROWN-OUT ACTUAL			66.0	V	Actual AC RMS brown-out threshold
<b>LINE OVERVOLTAGE</b>					
OVERVOLTAGE_LINE			304.2	V	Actual AC RMS line over-voltage threshold
<b>BIAS DIODE</b>					
VBIAS			12.0	V	Rectified bias voltage
VF_BIAS			0.70	V	Bias winding diode forward drop
VREVERSE_BIASDIODE			58.67	V	Bias diode reverse voltage (not accounting parasitic voltage ring)
CBIAS			22	uF	Bias winding rectification capacitor
CBPP			4.70	uF	BPP pin capacitor
<b>SECONDARY COMPONENTS</b>					
RFB_UPPER			100.00	kΩ	Upper feedback resistor (connected to the first output voltage)
RFB_LOWER			3.65	kΩ	Lower feedback resistor
CFB_LOWER			330	pF	Lower feedback resistor decoupling capacitor
<b>MULTIPLE OUTPUT PARAMETERS</b>					
<b>OUTPUT 1</b>					
VOU1			36.00	V	Output 1 voltage
IOU1			2.00	A	Output 1 current
POU1			72.00	W	Output 1 power
IRMS_SECONDARY1			3.352	A	Root mean squared value of the secondary current for output 1
IRIPPLE_CAP_OUTPUT1			2.690	A	Current ripple on the secondary waveform for output 1
AWG_SECONDARY1			21	AWG	Wire size for output 1
OD_SECONDARY1_INSULATED			1.029	mm	Secondary winding wire outer diameter with insulation for output 1
OD_SECONDARY1_BARE			0.723	mm	Secondary winding wire outer diameter without insulation for output 1
CM_SECONDARY1			670	Cmils	Bare conductor effective area in circular mils for output 1
NSECONDARY1			7		Number of turns for output 1
VREVERSE_RECTIFIER1			144.90	V	SRFET reverse voltage (not accounting parasitic voltage ring) for output 1
SRFET1	AUTO	Info	AON7254		The voltage stress (including the parasitic ring) on the secondary MOSFET selected may exceed the device BVDSS: pick a MOSFET with a higher BVDSS
VF_SRFET1			0.132	V	SRFET on-time drain voltage for output 1
VBREAKDOWN_SRFET1			150	V	SRFET breakdown voltage for output 1
RDSON_SRFET1			66.0	mΩ	SRFET on-time drain resistance at 25degC and VGS=4.4V for output 1
PO_TOTAL			72.00	W	Total power of all outputs
NEGATIVE OUTPUT	N/A		N/A		If negative output exists, enter the output number; e.g. If VO2 is negative output, select 2
<b>TOLERANCE ANALYSIS</b>					





USER_VAC	115		115	V	Input AC RMS voltage corner to be evaluated
USER_ILIMIT	TYP		2.130	A	Current limit corner to be evaluated
USER_LPRIMARY	TYP		552.3	uH	Primary inductance corner to be evaluated
MODE_OPERATION			CCM		Mode of operation
KP			0.858		Measure of continuous/discontinuous mode of operation
FSWITCHING			66983	Hz	Switching frequency at full load and valley of the rectified minimum AC input voltage
VMIN			139.50	V	Valley of the minimum input AC voltage at fullload
DUTYCYCLE			0.463		Steady state duty cycle
TIME_ON			7.73	us	Primary switch on-time
TIME_OFF			8.02	us	Primary switch off-time
IPEAK_PRIMARY			2.030	A	Primary switch peak current
IPEDESTAL_PRIMARY			0.289	A	Primary switch current pedestal
IAVERAGE_PRIMARY			0.537	A	Primary switch average current
IRIPPLE_PRIMARY			1.742	A	Primary switch ripple current
IRMS_PRIMARY			0.860	A	Primary switch RMS current
BPEAK			3216	Gauss	Peak flux density
BMAX			2995	Gauss	Maximum flux density
BAC			1285	Gauss	AC flux density (0.5 x Peak to Peak)

Note: The spreadsheet displays a warning for output voltage, as the specified 36V output is greater than the rating of the InnoSwitch Vout pin. This problem is addressed by using two stacked output voltage windings and feeding the Vout pin with the lower winding stack such that the voltage is with the ratings of the InnoSwitch Vout pin.

## 8 Transformer Specification

### 8.1 Electrical Diagram

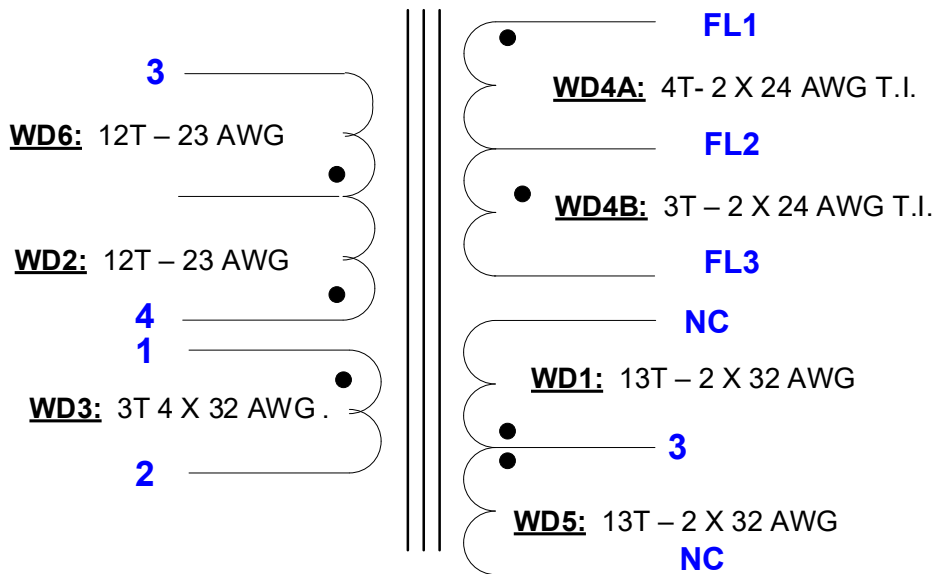


Figure 6 – Transformer Electrical Diagram.

### 8.2 Electrical Specifications

<b>Electrical Strength</b>	1 second, 60 Hz, from Pins 1-4 to FL1-3.	3000 VAC
<b>Primary Inductance</b>	Pins 3-4, all other windings open, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	552 μH, ±5%
<b>Resonant Frequency</b>	Pins 3-4, all other windings open.	600 kHz (Min.)
<b>Primary Leakage</b>	Pins 3-4, with FL1 and FL3 shorted, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	4 μH (Max.)

### 8.3 Material List

Item	Description
[1]	Core Pair: ATQ28-18, A <sub>LG</sub> of 958 nH/T <sup>2</sup> .
[2]	Bobbin: ATQ28-18 Vertical, 4 pins.
[3]	Triple Insulated Wire: #24 AWG Furukawa Tex-E or Equivalent.
[4]	Magnet Wire: #32 AWG Solderable Double Coated.
[5]	Magnet Wire: #25 AWG Solderable Double Coated.
[6]	Tape: Polyester Film, 3M 1350F-1 or Equivalent, 8.4 mm wide.
[7]	Tape: Polyester Film, 3M 1350F-1 or Equivalent, 30 mm Wide.
[8]	Varnish. Dolph BC-359 or Equivalent.

8.4 *Transformer Build Diagram*

**WD6:** 2<sup>nd</sup> primary 12 T – #23 AWG

**WD5:** Shield 13T – 2 X #32 AWG

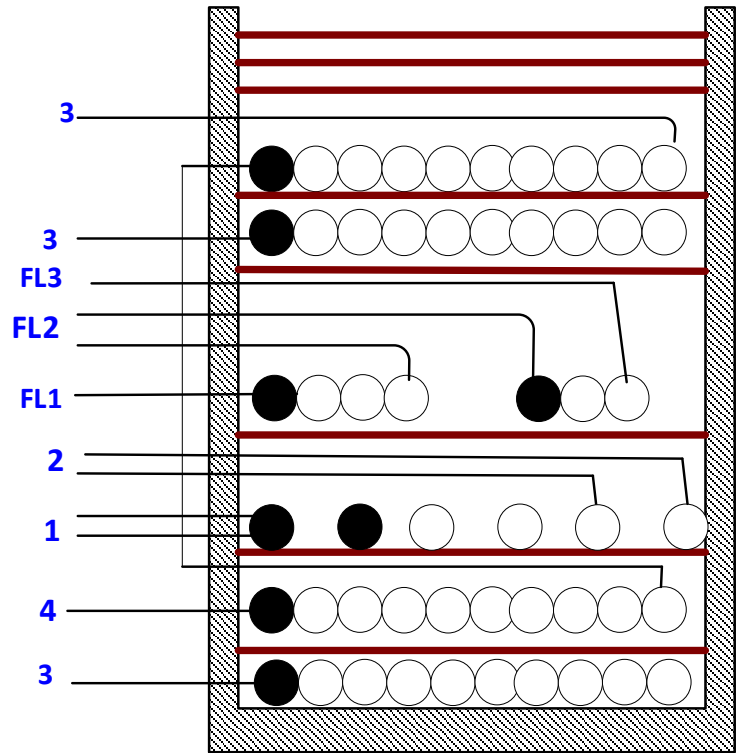
**WD4B:** Sec 3T – 2 X #24 AWG T.I.

**WD4A:** Sec 4T – 2 X #24 AWG T. I.

**WD3:** Bias 3T – 4 X #32 AWG

**WD2:** 1<sup>st</sup> Primary 12T – #23 AWG

**WD1:** Shield 13T – 2 X #32 AWG



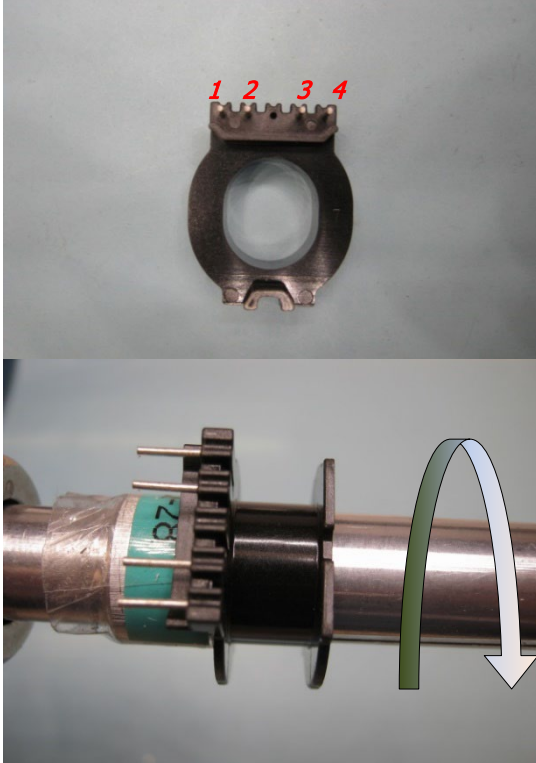
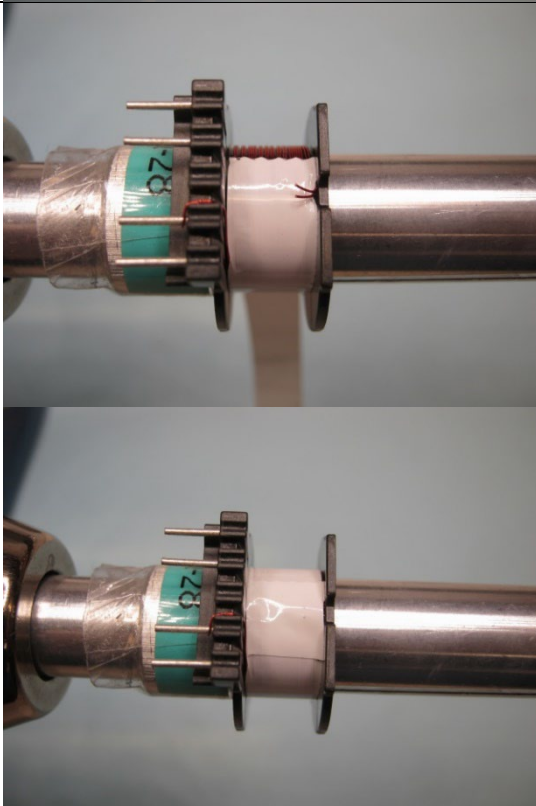
**Figure 7** – Transformer Build Diagram.

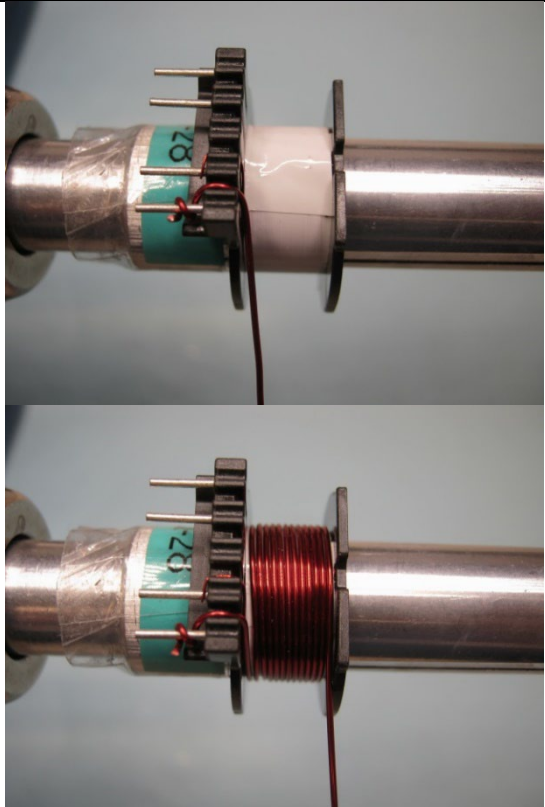
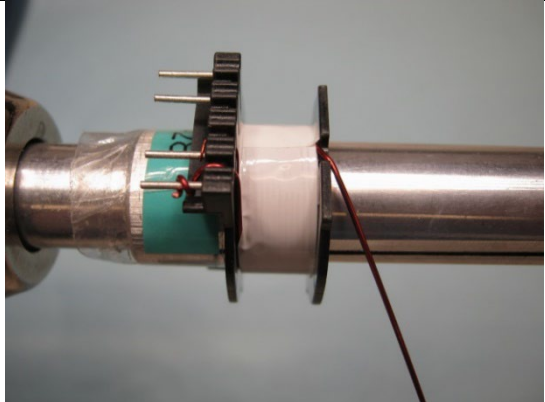
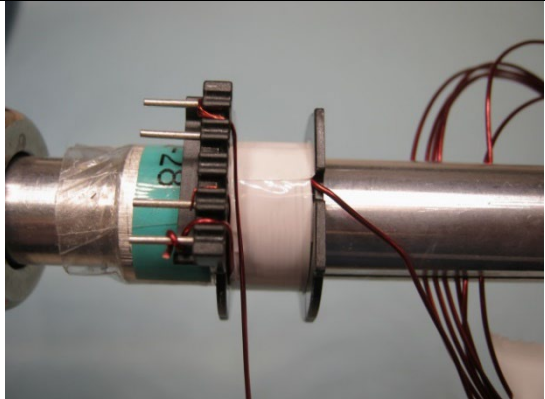


## 8.5 Transformer Construction

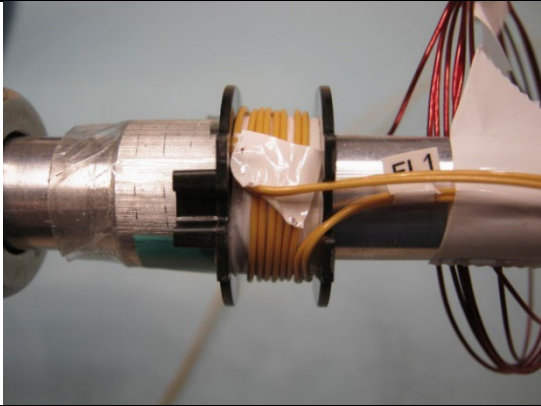
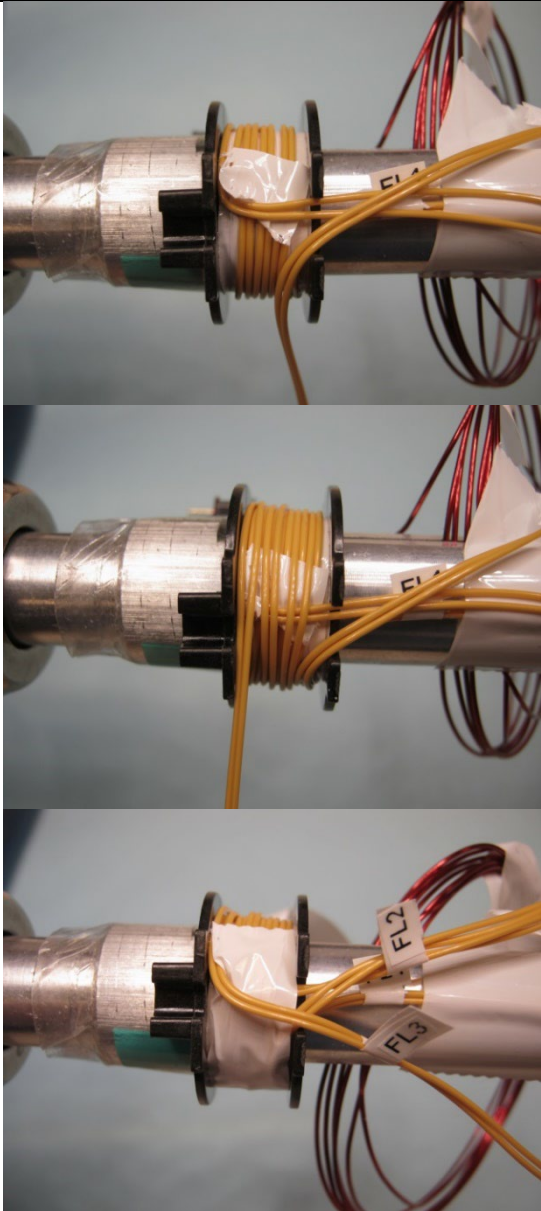
<b>Winding Preparation</b>	Position the bobbin Item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.
<b>WD1 Shield/Insulation</b>	Starting at pin 3, wind 13 bifilar turns of wire Item [4] in one layer. Place 1.5 layer of tape Item [6]. Cut finish lead of previous winding short, trap between tape layers.
<b>WD2 1<sup>st</sup> half Primary</b>	Starting at Pin 4, wind 12 turns of magnet wire Item [5] in 1 layer with tight tension. Bring out finish wire on non-pin side with enough length for 2 <sup>nd</sup> primary layer.
<b>Insulation</b>	Place 1 layer of tape Item [6].
<b>WD3 Bias</b>	Starting at pin 1, wind 3 quadriifilar turns of wire Item [4] in 1 layer, spread wire evenly on the bobbin, and finish at pin 2.
<b>Insulation</b>	Place 1 layer of tape Item [6].
<b>WD5 Shield/Insulation</b>	Starting at pin 3, wind 13 bifilar turns of wire Item [4] in 1 layer with tight tension Use 1.5 turns of tape to secure winding – bury finish between tape layers.
<b>WD4A Secondary</b>	Start with _ cm bifilar length of TIW Item [3] with 3 cm flying start lead exiting from secondary winding slot opposite to bobbin pin side per picture. Tape to mandrel as shown. Mark start lead. Wind 4 bifilar turns of TIW Item [3], bring finish back to secondary slot as shown. Leave 3 cm of finish lead, tape to mandrel to secure.
<b>WD4B Secondary</b>	Start with _ cm bifilar length of TIW with 3 cm flying start lead exiting from secondary winding slot as shown. Tape start lead to mandrel as shown. Mark start lead. Wind 3 bifilar turns of TIW Item [3], bring finish back to secondary slot. Leave 3 cm of finish lead, tape to mandrel to secure.
<b>Insulation</b>	Place 2 layers of tape Item [6].
<b>WD5 Shield/Insulation</b>	Starting at pin 3, wind 13 bifilar turns of wire Item [4] in 1 layer with tight tension Use 1.5 turns of tape to secure winding – bury finish between tape layers.
<b>Insulation</b>	Place 1 layer of tape Item [6].
<b>WD6 2<sup>nd</sup> half Primary</b>	Starting with wire left from first primary layer, wind 12 bifilar turns of wire Item [5] in 1 layer with tight tension, and finish at pin 3.
<b>Finish Wrap</b>	Place 3 layers of tape Item [6].
<b>Finish</b>	Gap core halves for 552 $\mu$ H $\pm$ 5%. Assemble core halves in bobbin, secure with two turns of tape Item [6]. Wrap secondary side of assembled transformer as shown with 3 layers of tape Item [7] as shown. Secure tape wrap with 3 turns of tape Item [6] as shown. Twist finish of WDG 4A and start of WDG 4B together, trim to 30 mm and tin 5 mm. Twist WDG 4A start wires together, trim to 30mm and tin 5 mm. Twist finish leads of WD 4B tightly together, trim to 30 mm and tin 5 mm. Dip varnish Item [8].

8.6 *Winding Illustrations*

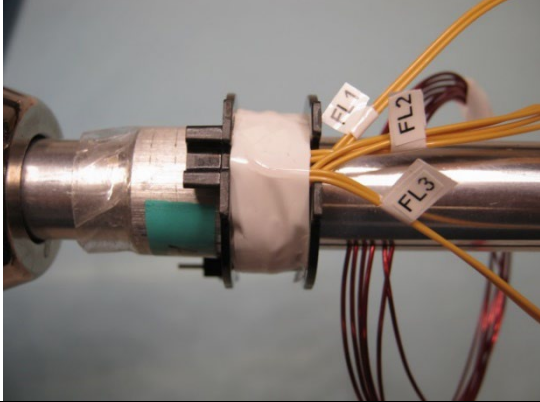
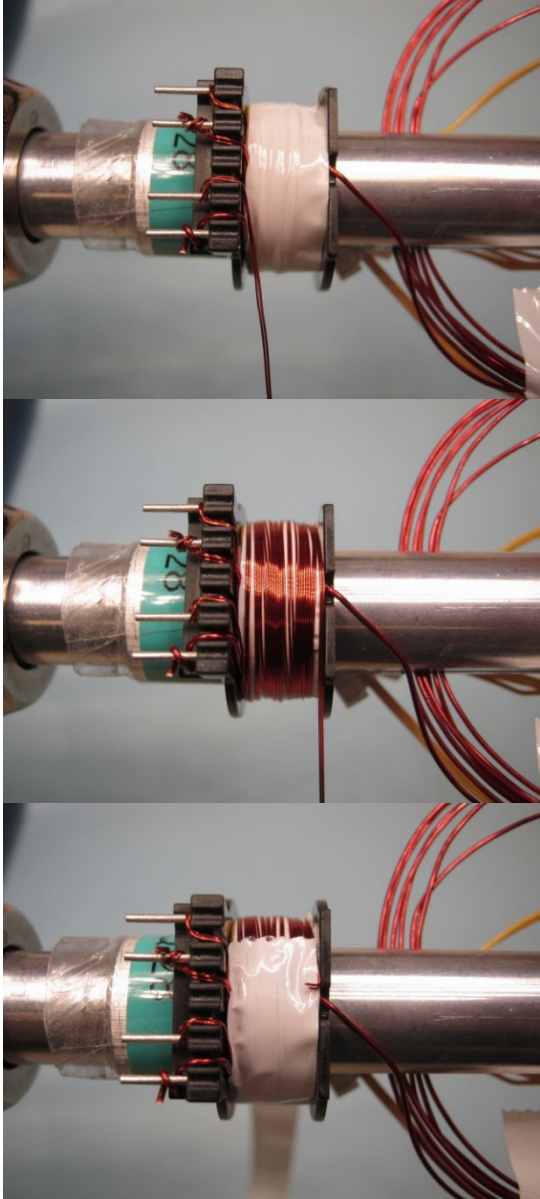
<p><b>Winding Preparation</b></p>		<p>Pin-out of bobbin is indicated as in picture beside. Position the bobbin Item [2] on the mandrel such that the pin side is on the left. Winding direction is clock-wise direction.</p>
<p><b>WD1 Shield/Insulation</b></p>		<p>Starting at pin 3, wind 13 bifilar turns of wire Item [4] in one layer. Place 1.5 layer of tape Item [6]. Cut finish lead of previous winding short, trap between tape layers.</p>

<p><b>WD2</b> <b>1/2 Primary</b></p>		<p>Starting at Pin 4, wind 12 turns of magnet wire Item [5] in 1 layer with tight tension. Bring out finish wire on non-pin side with enough length for 2<sup>nd</sup> primary layer.</p>
<p><b>Insulation</b></p>		<p>Place 1 layer of tape Item [6].</p>
<p><b>WD3</b> <b>Bias</b></p>		<p>Starting at pin 1, wind 3 quadfil turns of wire Item [4] in 1 layer, spread wire evenly on the bobbin, and finish at pin 2.</p>

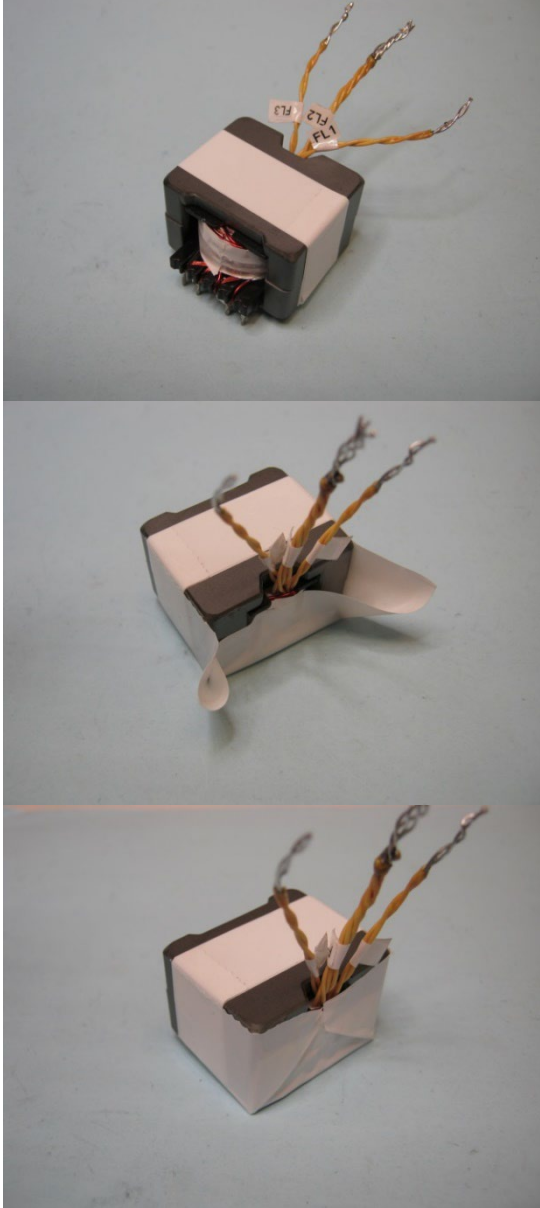
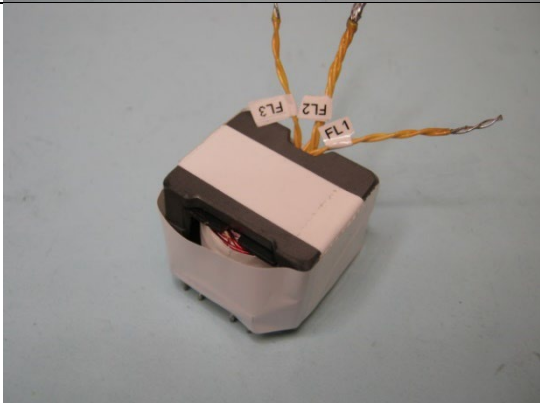
<p><b>Insulation</b></p>		<p>Place 1 layer of tape Item [6].</p>
<p><b>WD4A Secondary</b></p>		<p>Start with <u>  </u>cm bifilar length of TIW Item [3] with 3 cm flying start lead exiting from secondary winding slot opposite to bobbin pin side per picture. Tape to mandrel as shown. Mark start lead. Wind 4 bifilar turns of TIW Item [3], place a piece of to hold wires in place then bring finish back to secondary slot as shown. Leave 3 cm of finish lead, tape to mandrel to secure.</p>

		
<p><b>WD4b Secondary</b></p>		<p>Start with _ cm bifilar length of TIW with 3 cm flying start lead exiting from secondary winding slot as shown. Tape start lead to mandrel as shown. Mark start lead. Wind 3 bifilar turns of TIW Item [3], bring finish back to secondary slot. Leave 3 cm of finish lead, tape to mandrel to secure.</p>



<p><b>Insulation</b></p>		<p>Place 1 layer of tape Item [6].</p>
<p><b>WD5 Shield/Insulation</b></p>		<p>Starting at pin 3, wind 13 bifilar turns of wire Item [4] in 1 layer with tight tension Use 1.5 turns of tape to secure winding – bury finish between tape layers</p>

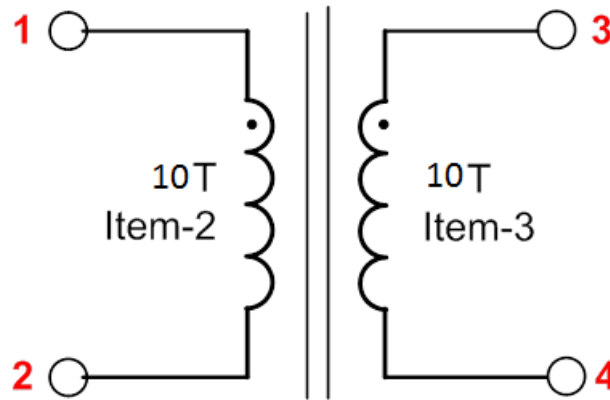
<p><b>WD6</b> <b>2<sup>nd</sup> half Primary</b></p>		<p>Starting with wire left from first primary layer, wind 12 bifilar turns of wire Item [5] in 1 layer with tight tension, and finish at pin 3.</p>
<p><b>Finish Wrap</b></p>		<p>Place 3 layers of tape Item [6].</p>

<p><b>Finish</b></p>		<p>Gap core halves for 552 <math>\mu</math>H <math>\pm</math>5%. Assemble core halves in bobbin, secure with two turns of tape Item [6]. Wrap secondary side of assembled transformer as shown with 3 layers of tape Item [7]. Secure tape wrap with 3 turns of tape Item [6] as shown. Twist finish of WDG 4A and start of WDG 4B together, trim to 30 mm and tin 5 mm. Twist WDG 4A start wires together, trim to 30mm and tin 5 mm. Twist finish leads of WD 4B tightly together, trim to 30 mm and tin 5 mm. Dip varnish Item [8].</p>
		<p>Finished transformer.</p>

## 9 Input HF Common Mode Choke Specifications

### 9.1 250 $\mu$ H Common Mode Choke (L3)

#### 9.1.1 Electrical Diagram



**Figure 8** – Inductor Electrical Diagram.

#### 9.1.2 Electrical Specifications

<b>Winding Inductance</b>	Pin 1 – pin 2 (pin 3 – pin 4), all other windings open, measured at 100 kHz, 0.4 V <sub>RMS</sub> .	250 $\mu$ H $\pm$ 20%
---------------------------	---	-----------------------

#### 9.1.3 Material List

Item	Description
[1]	Toroidal Core: 35T0375-10H, PI#: 32-00275-00.
[2]	Triple Insulated Wire: #27 AWG, Triple Coated.
[3]	Magnet Wire: #27 AWG, Double Coated.



**Figure 9**– Finished Choke.

### 10 U1 Heat Sink

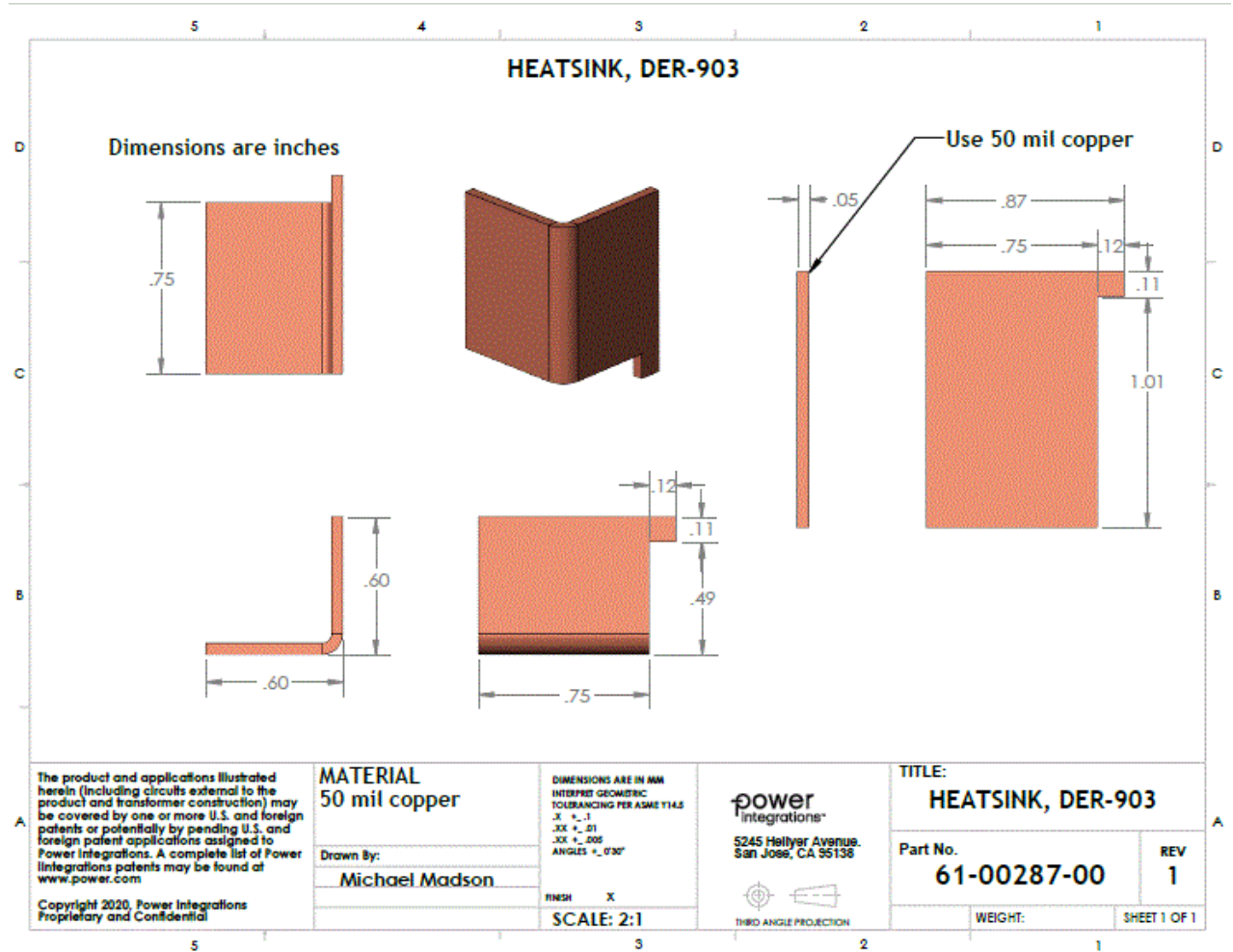


Figure 10 – U1 Heat Sink.



### 11 Performance Data

All the performance data have been taken at the board output terminals unless otherwise specifically mentioned.

#### 11.1 Efficiency vs. Load

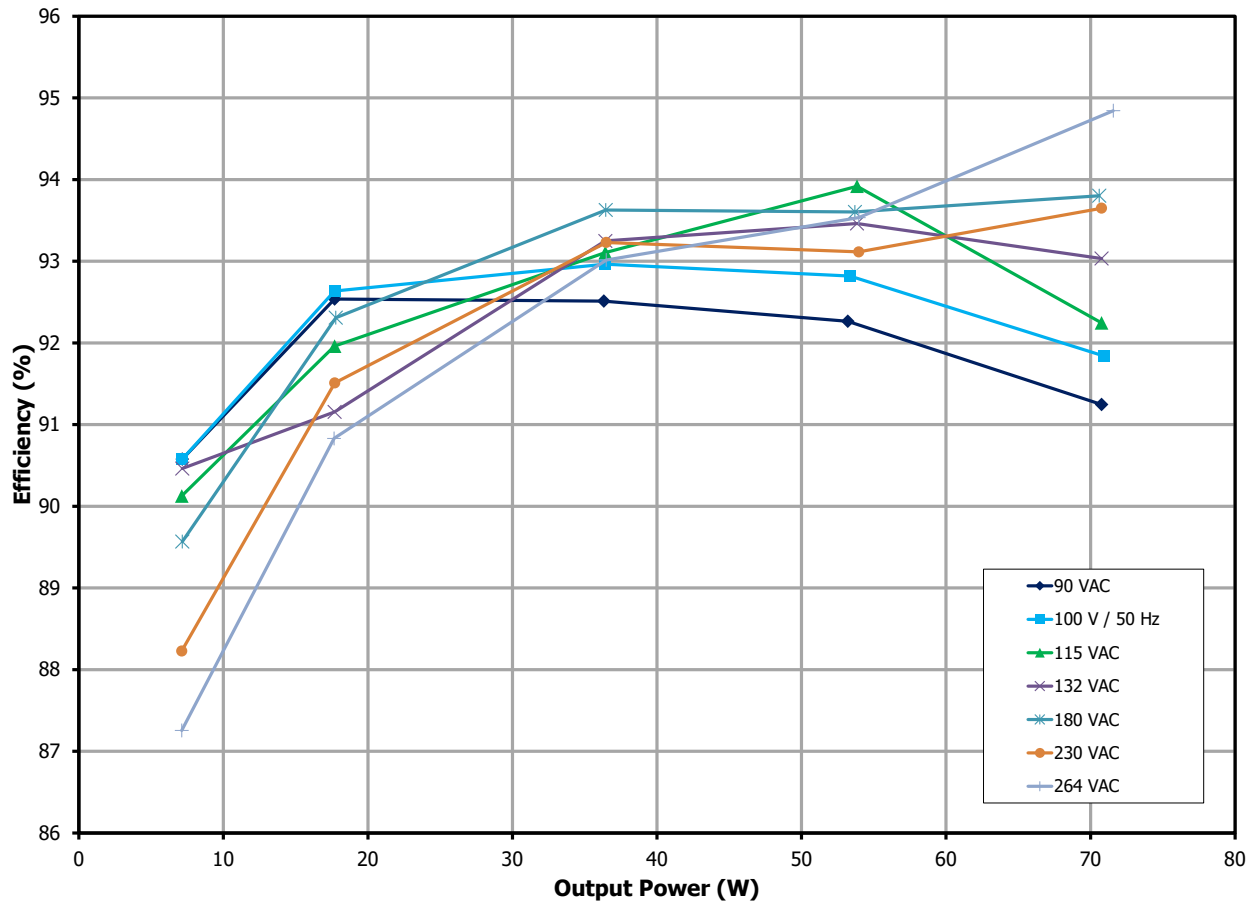


Figure 11 – Efficiency vs. Load, Room Ambient.

### 11.2 No-Load Input Power

No-load power was measured using a Yokogawa WT210 operating in watt-seconds mode, with 20 minute integration time.

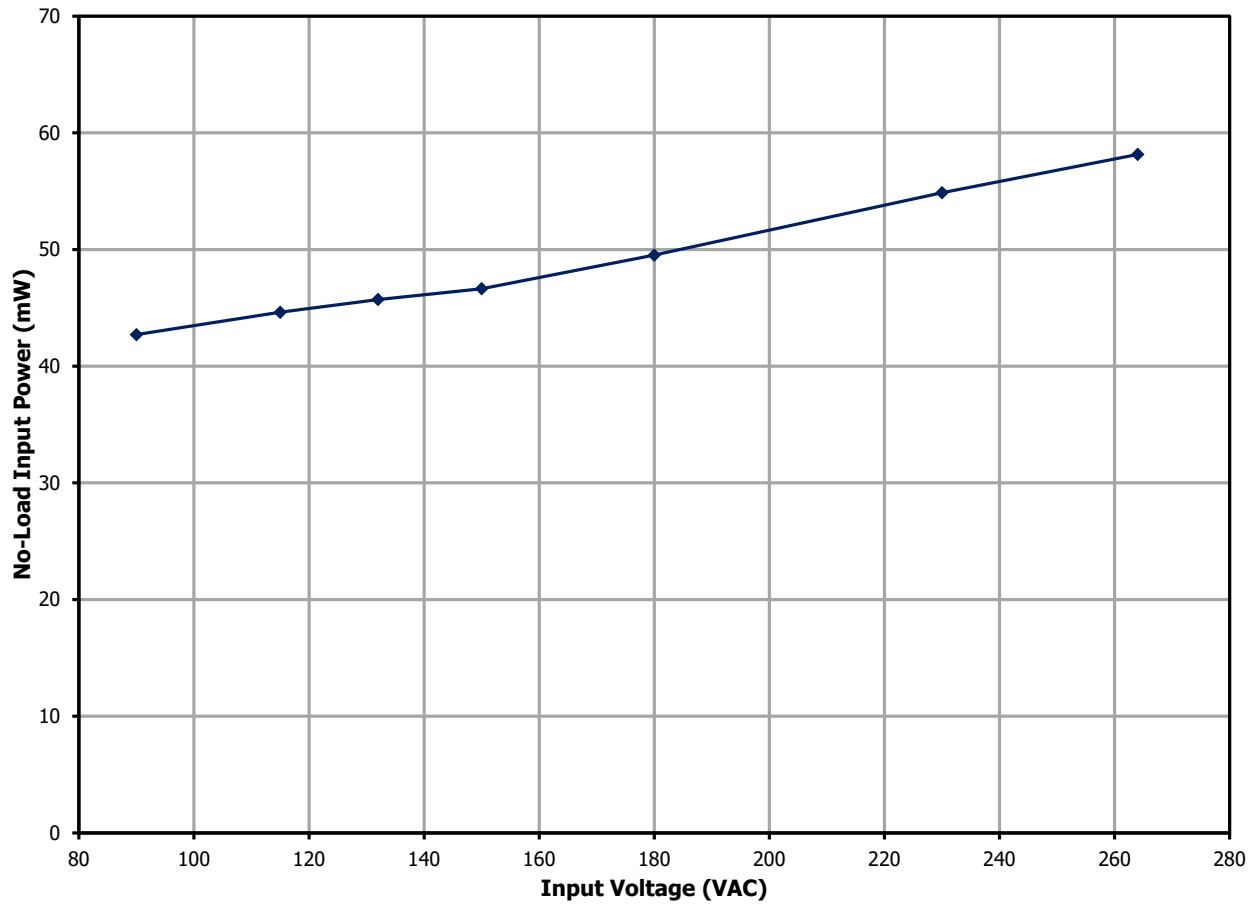


Figure 12 – No-Load Input Power vs. Input Line Voltage, Room Temperature.



### 11.3 Line Regulation

Line regulation data was captured at supply output terminals.

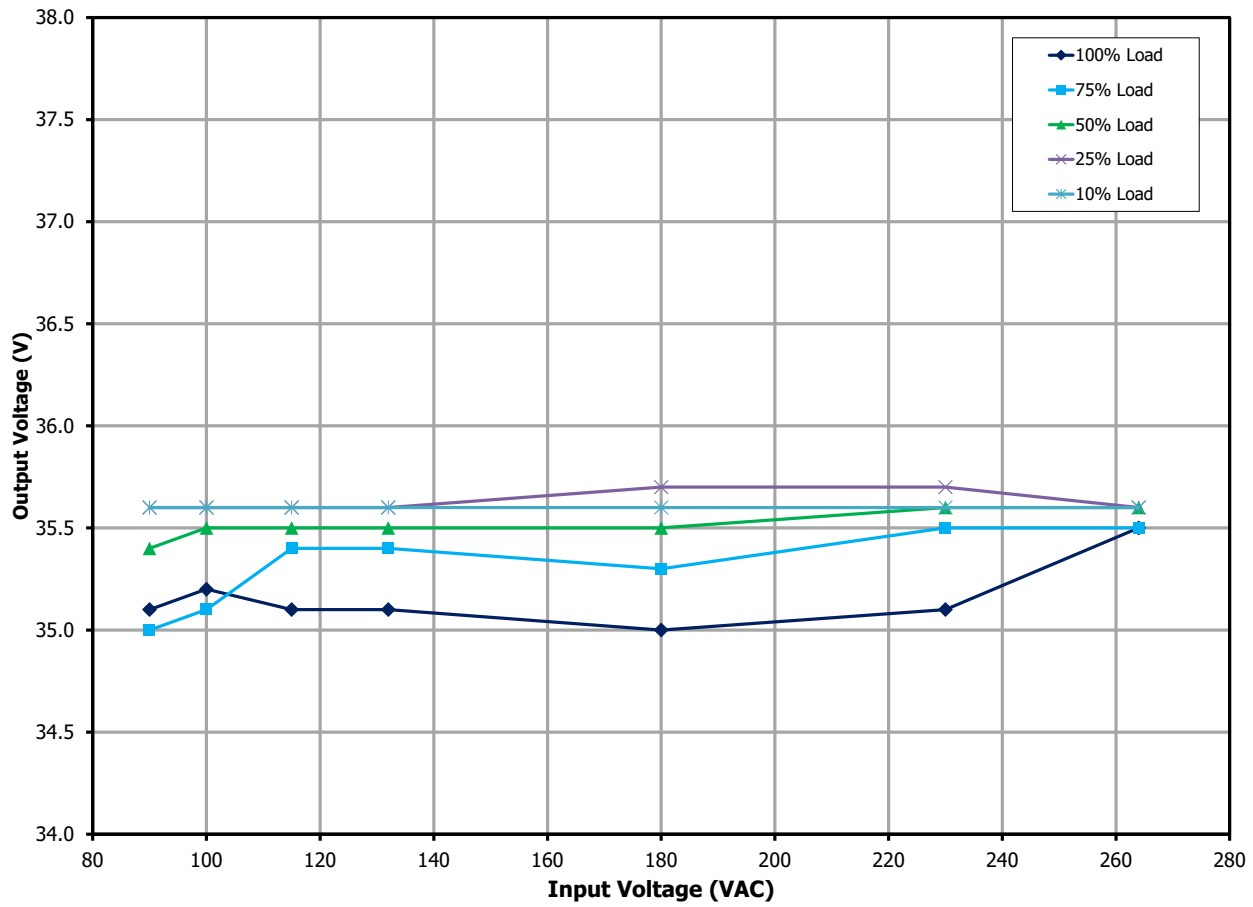


Figure 13 – Line Regulation, Room Temperature



### 11.4 Load Regulation

Load regulation data was captured at supply output terminals.

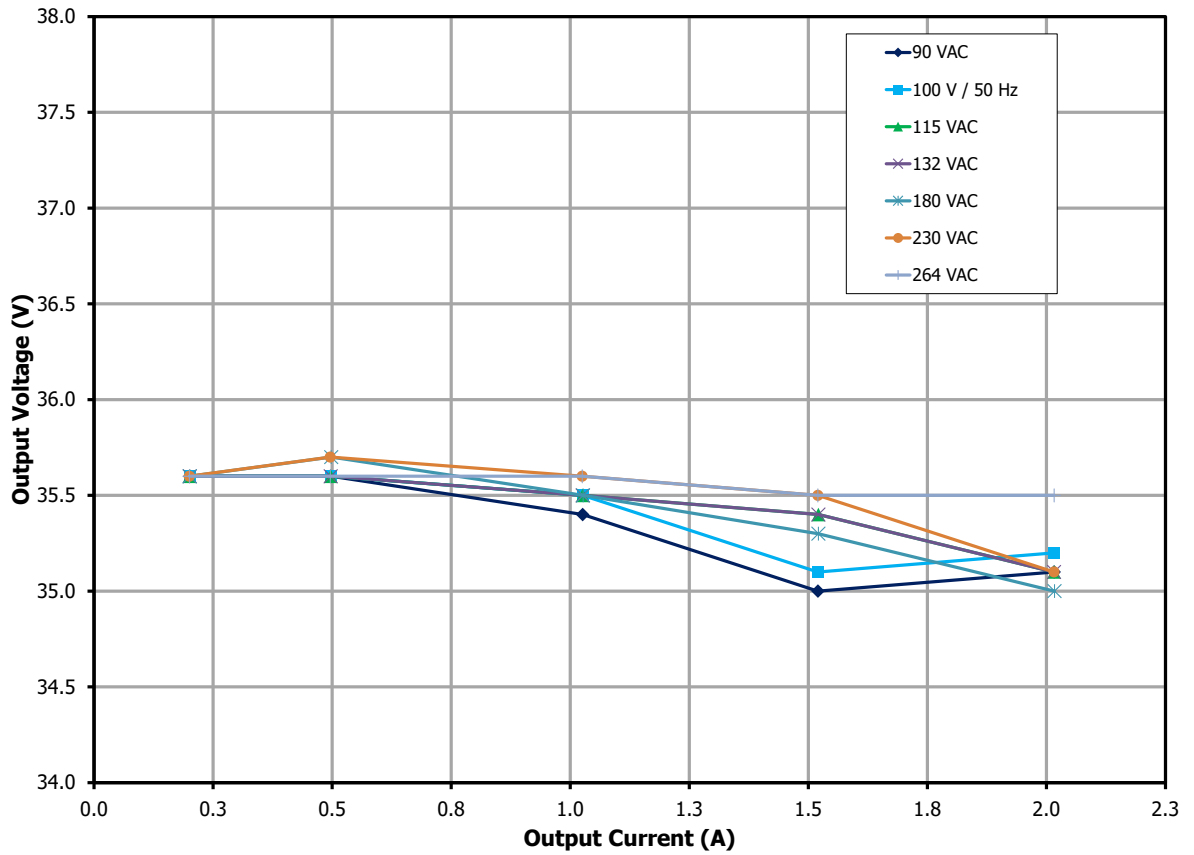


Figure 14 – Load Regulation, Room Temperature.



### 11.5 V-I Characteristic

The V-I characteristic was measured using an electronic load set to constant resistance, to plot the V-I characteristic in both the constant voltage and constant current region.

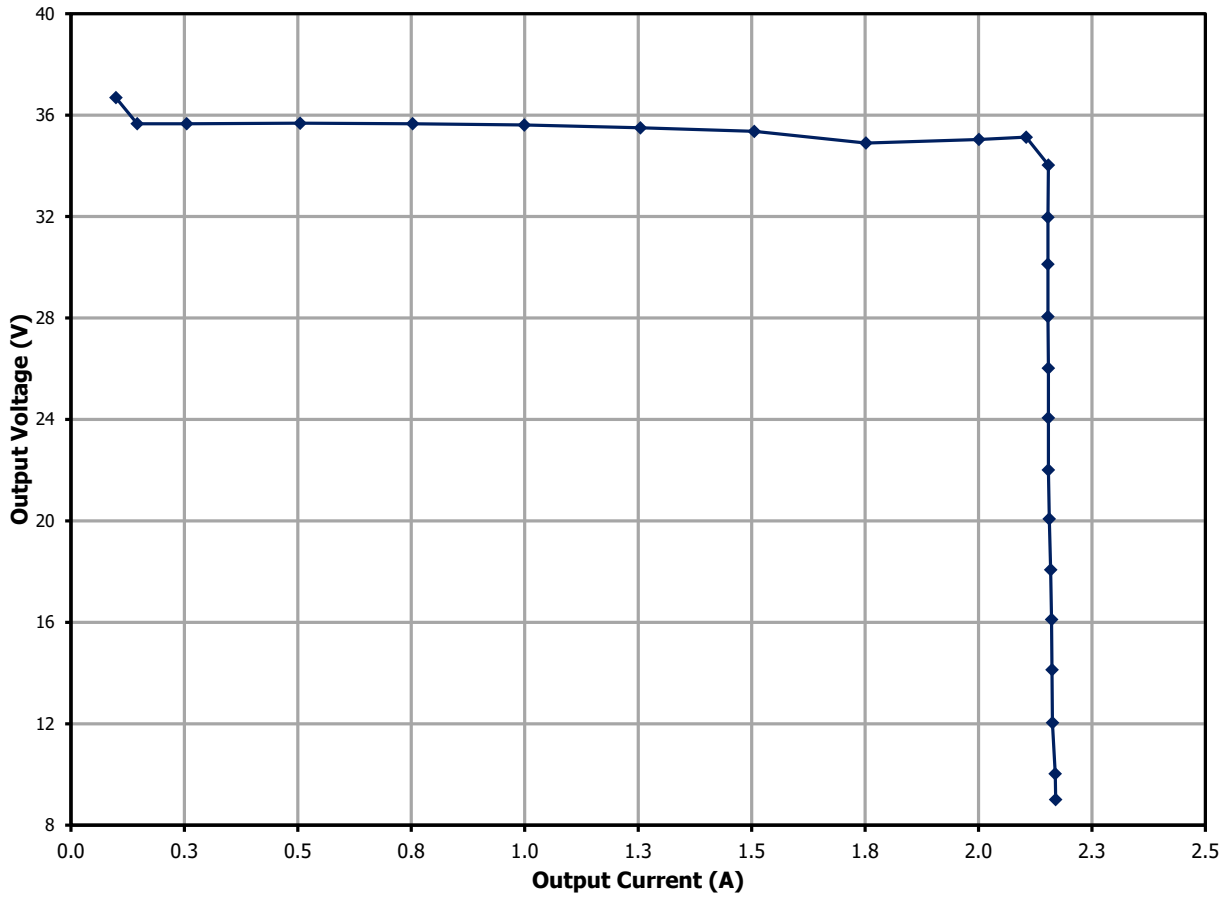


Figure 15 – V-I Characteristic, 115 VAC Input.

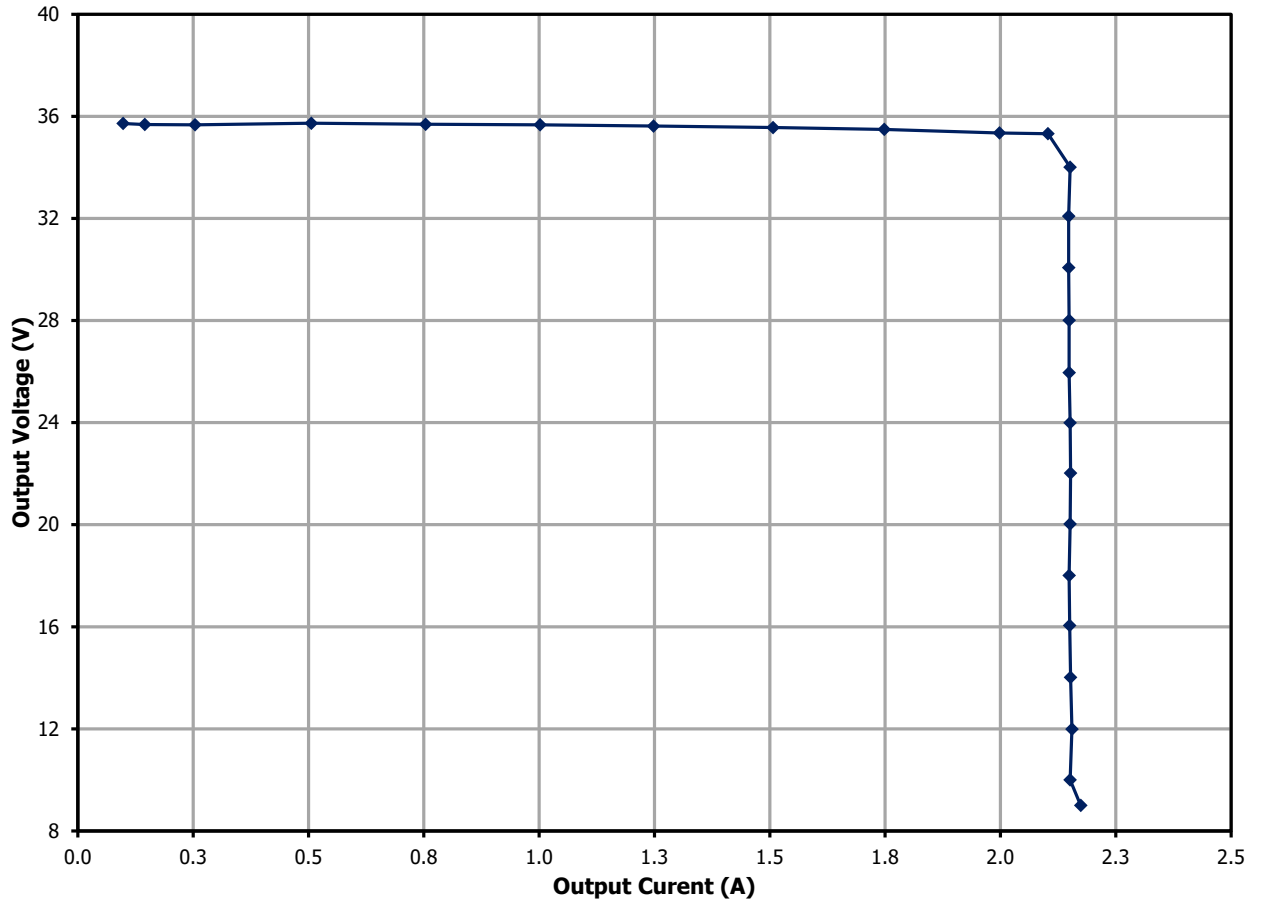


Figure 16 – V-I Characteristic, 230 VAC Input.



## 11.6 *Average Efficiency*

### 11.6.1 115 VAC

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%)</b>
100	70.76	92.25	<b>92.81</b>
75	53.84	93.92	
50	36.42	93.11	
25	17.69	91.96	

### 11.6.2 230 VAC

<b>% Load</b>	<b>P<sub>OUT</sub> (W)</b>	<b>Efficiency (%)</b>	<b>Average Efficiency (%)</b>
100	70.76	93.65	<b>92.88</b>
75	53.96	93.11	
50	36.49	93.23	
25	17.71	91.51	

### 11.7 Thermal Performance

Thermal performance is measured room temperature.

#### 11.7.1 90 VAC, 100% Load

90 VAC						
Amb	U1	Q1	D5	R19	T1 Core	T1 Wdg
26	89.8	72.6	91.9	74.5	72	81.7
<b>BR1</b>						
85.2						

#### 11.7.2 115 VAC, 100% Load

115 VAC						
Amb	U1	Q1	D5	R19	T1 Core	T1 Wdg
26	80.4	70.6	89.8	67.6	69.8	80.3
<b>BR1</b>						
72.8						

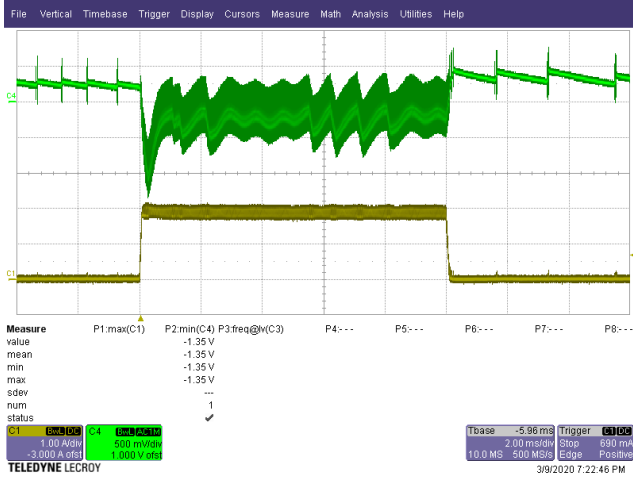
#### 11.7.3 230 VAC, 100% Load

230 VAC						
Amb	U1	Q1	D5	R19	T1 Core	T1 Wdg
26	57.4	63.7	86.9	69.9	70.1	78.9
<b>BR1</b>						
52.4						

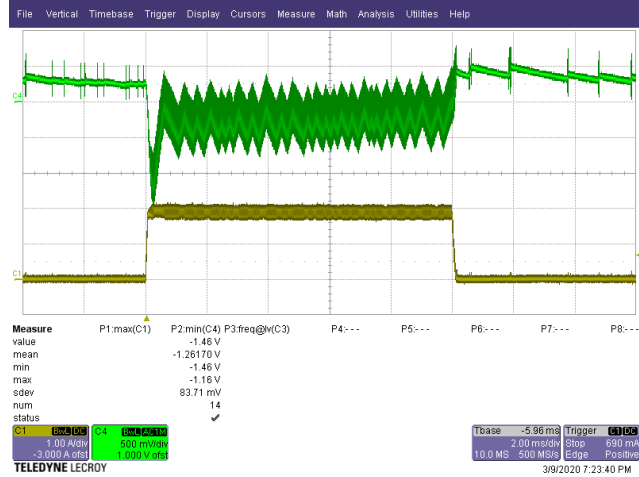
## 12 Waveforms

### 12.1 Load Transient Response (at output terminals)

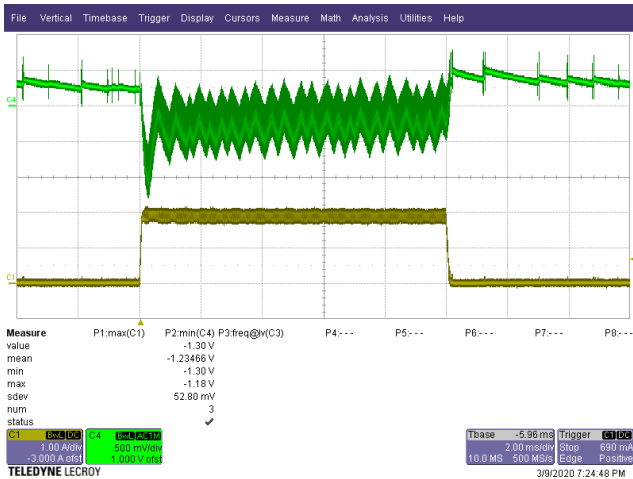
#### 12.1.1 0-100% Load Transient



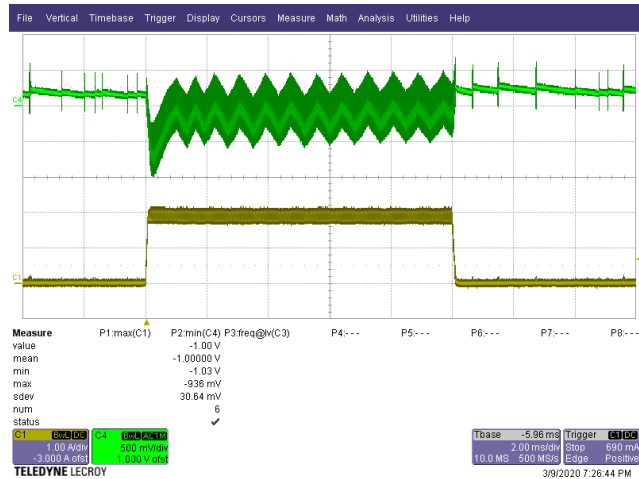
**Figure 17** – Transient Response 90 VAC, 0 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 500 mV / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.



**Figure 18** – Transient Response, 115 VAC, 0 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 500 mV / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

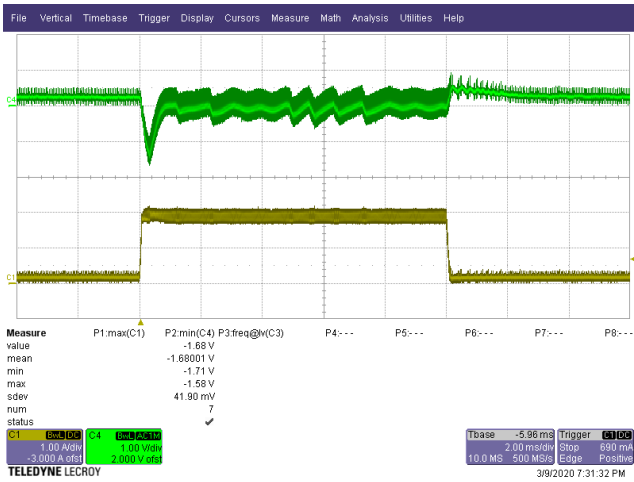


**Figure 19** – Transient Response, 230 VAC, 0 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 500 mV / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

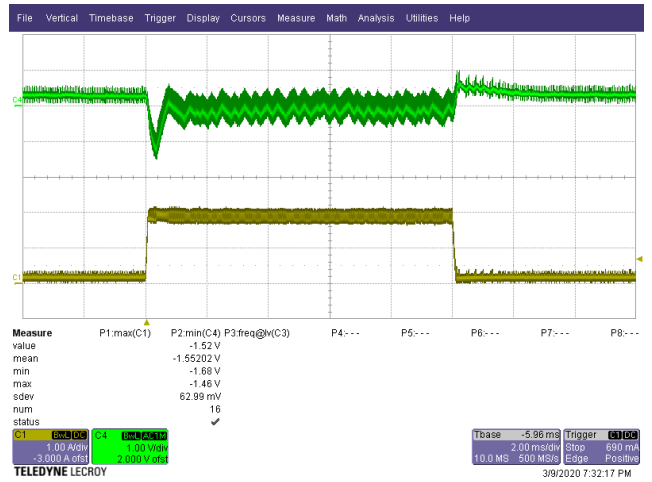


**Figure 20** – Transient Response, 264 VAC, 0 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 500 mV / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

### 12.1.2 10%-100% Load Transient

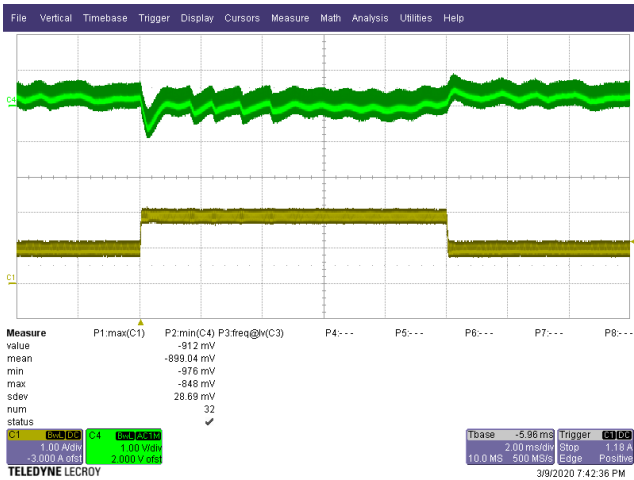


**Figure 21** – Transient Response, 90 VAC, 0.2 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 1 V / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

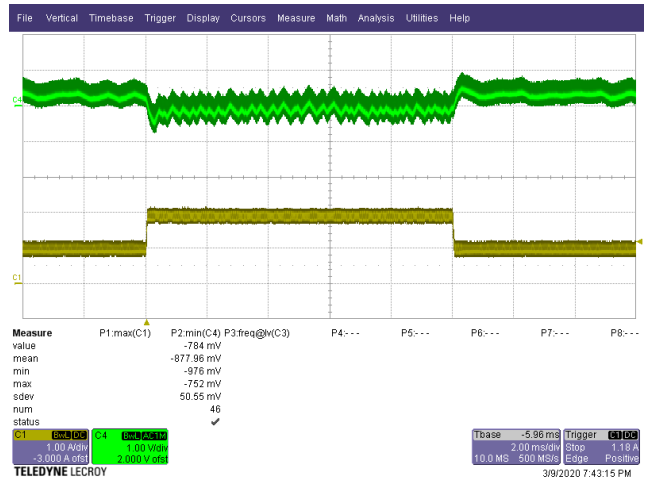


**Figure 22** – Transient Response, 115 VAC, 0.2 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 1 V / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

### 50%-100% Load Transient

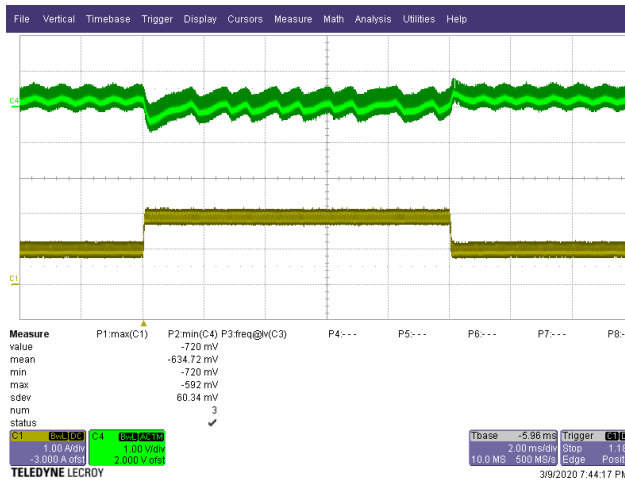


**Figure 23** – Transient Response, 90 VAC, 1 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 1 V / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

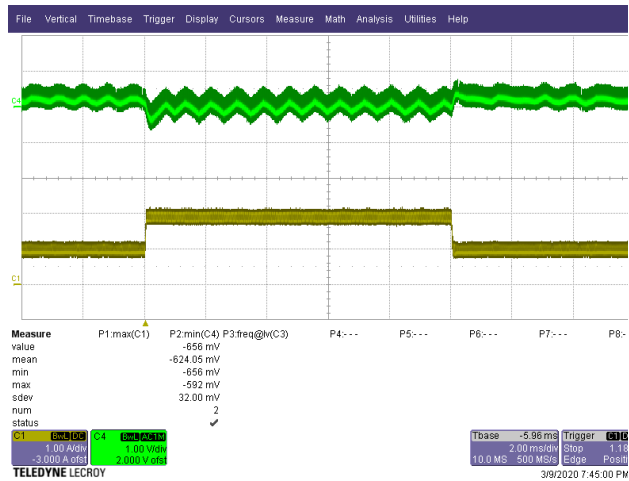


**Figure 24** – Transient Response, 115 VAC, 1 - 2 A Load Step.  
Upper:  $V_{OUT}$ , 1 V / div.  
Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.





**Figure 25** – Transient Response, 230 VAC, 1 - 2 A Load Step.  
 Upper:  $V_{OUT}$ , 1 V / div.  
 Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

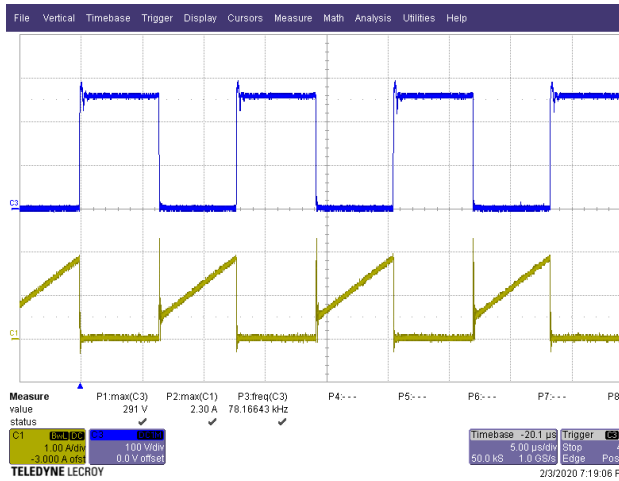


**Figure 26** – Transient Response, 264 VAC, 1 - 2 A Load Step.  
 Upper:  $V_{OUT}$ , 1 V / div.  
 Lower:  $I_{LOAD}$ , 1 A, 2 ms / div.

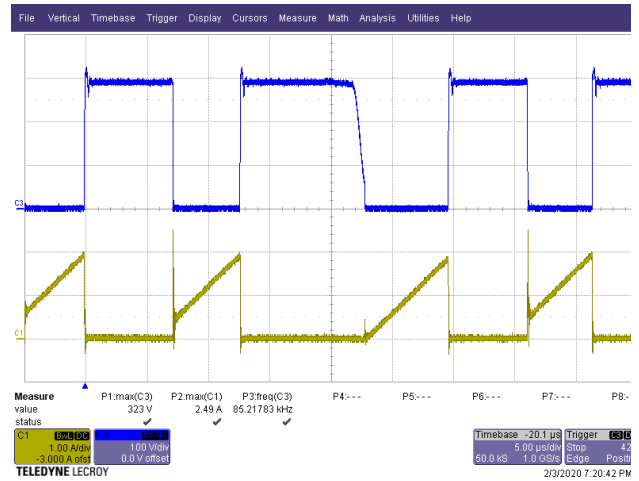


## 12.2 Switching Waveforms

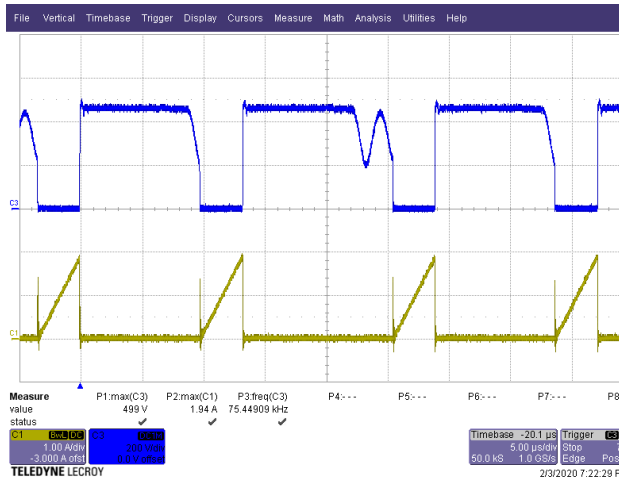
### 12.2.1 Primary Drain Voltage and Current



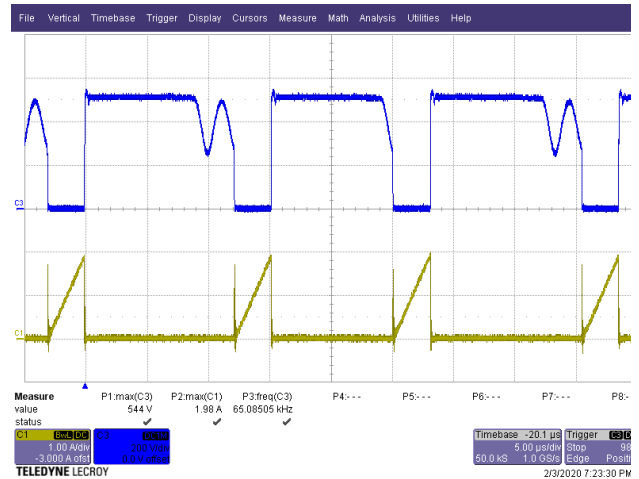
**Figure 27** – Flyback Drain Voltage and Current, 90 VAC Input, 2 A Load.  
Upper: Drain Voltage, 100 V / div.  
Lower: Drain Current, 1 A, 5 μs / div.



**Figure 28** – Flyback Drain Voltage and Current, 115 VAC Input, 2 A Load.  
Upper: Drain Voltage, 100 V / div.  
Lower: Drain Current, 1 A, 5 μs / div.



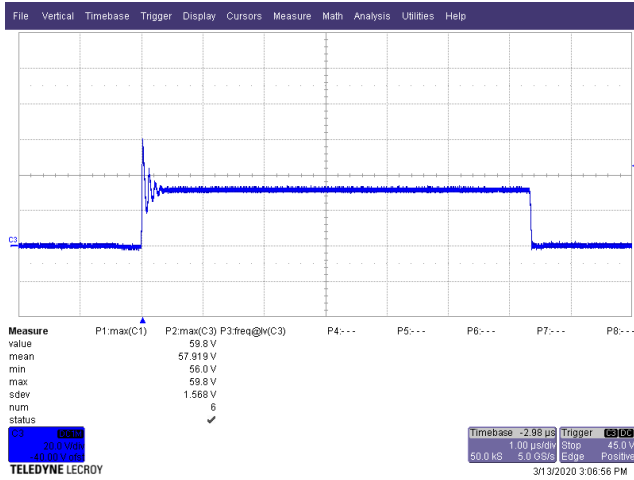
**Figure 29** – Flyback Drain Voltage and Current, 230 VAC Input, 2 A Load.  
Upper: Drain Voltage, 200 V / div.  
Lower: Drain Current, 1 A, 5 μs / div.



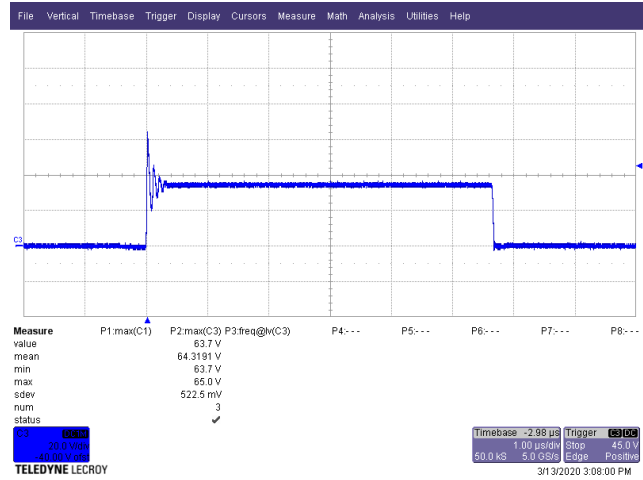
**Figure 30** – Flyback Drain Voltage and Current, 264 VAC Input, 2 A Load.  
Upper: Drain Voltage, 200 V / div.  
Lower: Drain Current, 1 A, 5 μs / div.

### 12.2.2 SR FET Voltage

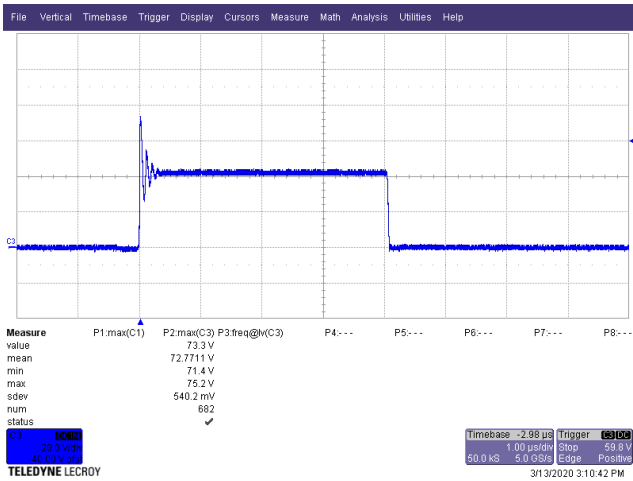
The reading taken at 168 V represents a worst-case situation, as it is the highest voltage where the supply still operates occasionally in continuous mode.



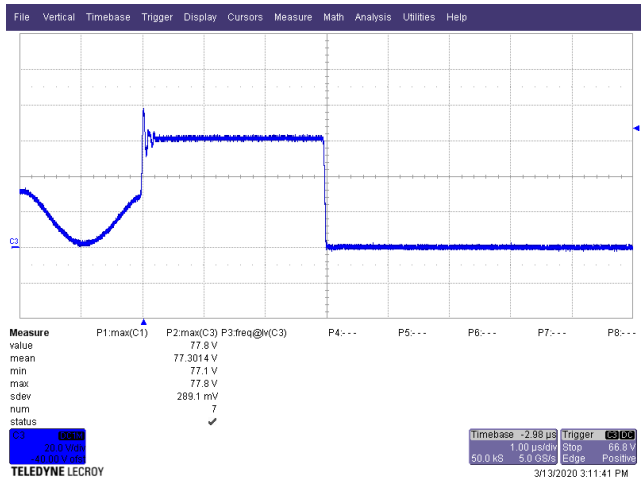
**Figure 31** – SR FET  $V_{DS}$ , 90 VAC, 2 A Load.  
 Blu - SR\_VDRAIN, 20 V, 1  $\mu$ s / div.



**Figure 32** – SR FET  $V_{DS}$ , 115 VAC, 2 A Load.  
 Blu - SR\_VDRAIN, 20 V / div, 1  $\mu$ s / div.



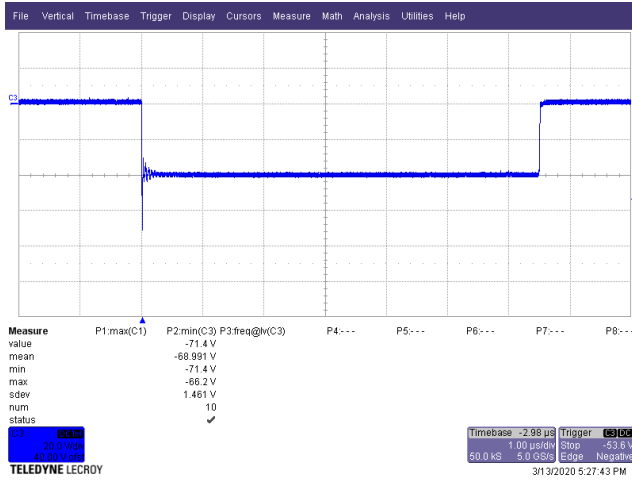
**Figure 33** – SR FET  $V_{DS}$ , 168 VAC, 2 A Load.  
 Blu - SR\_VDRAIN, 20 V / div, 1  $\mu$ s / div.



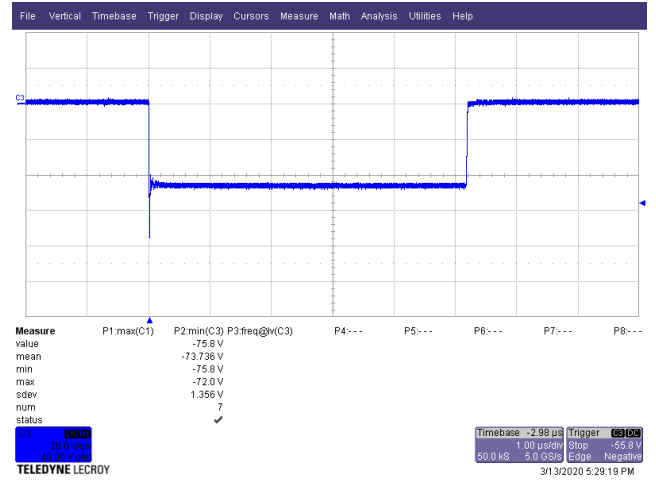
**Figure 34** – SR FET  $V_{DS}$ , 264 VAC, 2 A Load.  
 Blu - SR\_VDRAIN, 20 V / div, 1  $\mu$ s / div.

### 12.2.3 Diode (D5) Voltage

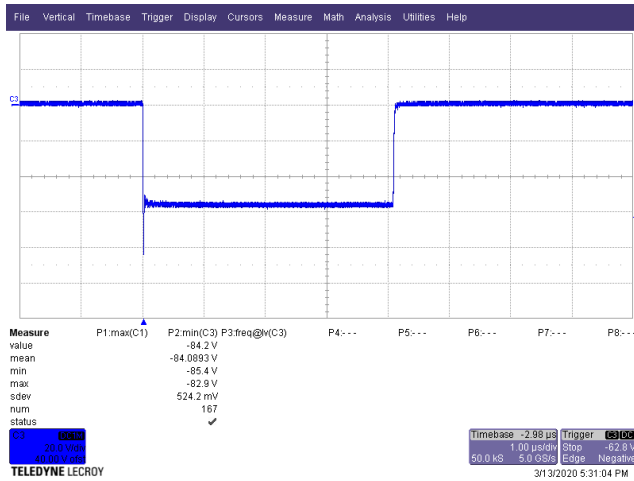
The reading taken at 169 V represents a worst-case situation, as it is the highest voltage where the supply still operates occasionally in continuous mode.



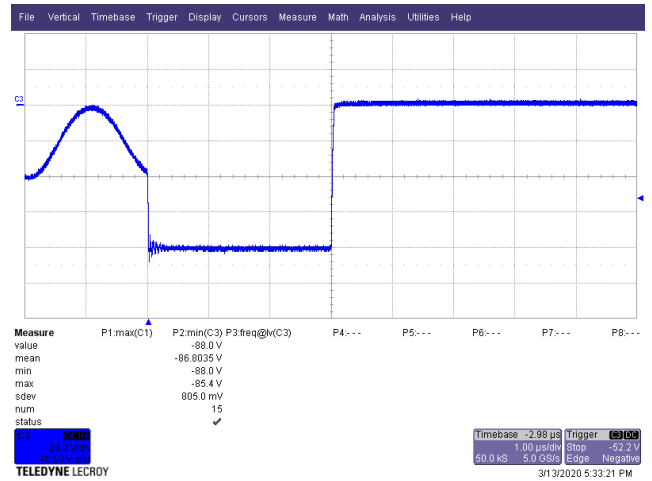
**Figure 35** – D5 PIV, 90 VAC, 2 A Load.  
 Blu – D9 PIV, 20 V / 1  $\mu$ s / div.



**Figure 36** – D5 PIV, 115 VAC, 2 A Load.  
 Blu – D9 PIV, 20 V / 1  $\mu$ s / div.



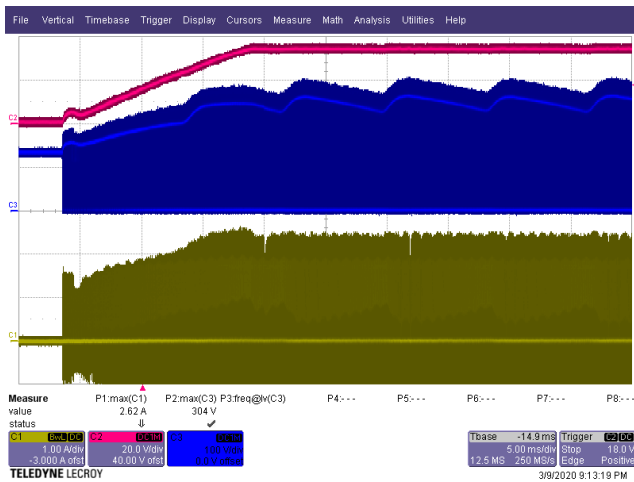
**Figure 37** – D5 PIV, 169 VAC, 2 A Load.  
 Blu - D9 PIV, 20 V / 1  $\mu$ s / div.



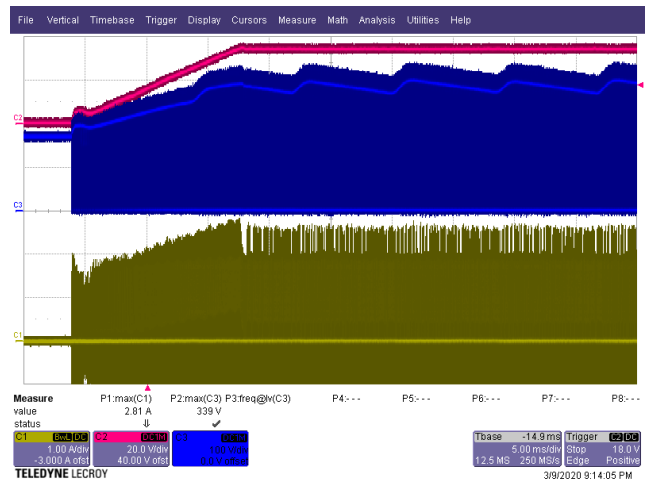
**Figure 38** – D5 PIV, 264 VAC, 2 A Load.  
 Blu – D9 PIV, 20 V / 1  $\mu$ s / div.



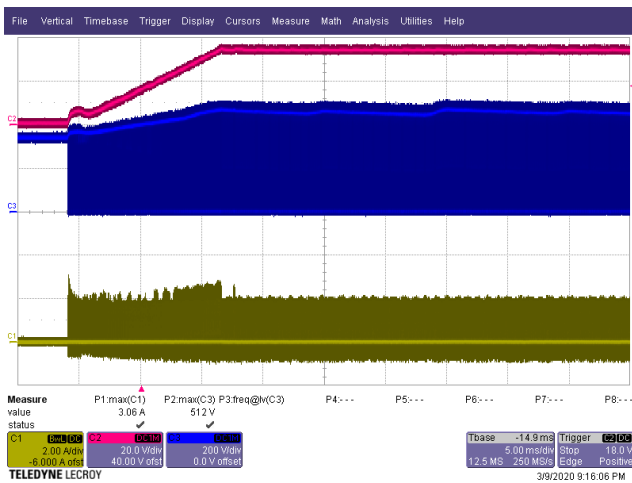
### 12.2.4 Flyback Start-up Waveforms



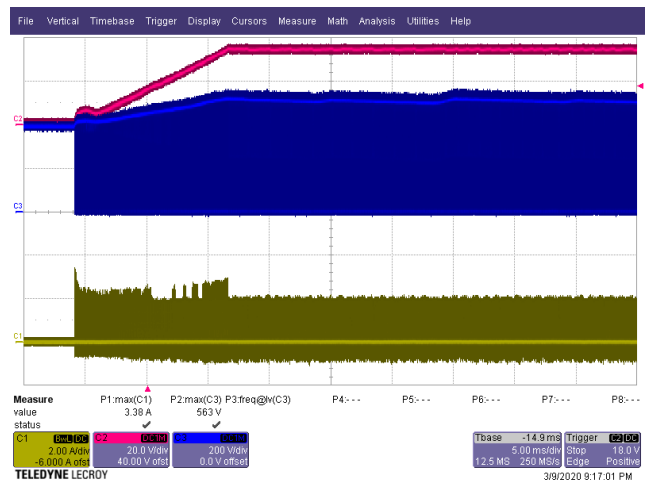
**Figure 39** – Flyback Start-up Waveforms, 90 VAC Input, 2 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 100 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 1 A, 5 ms / div.



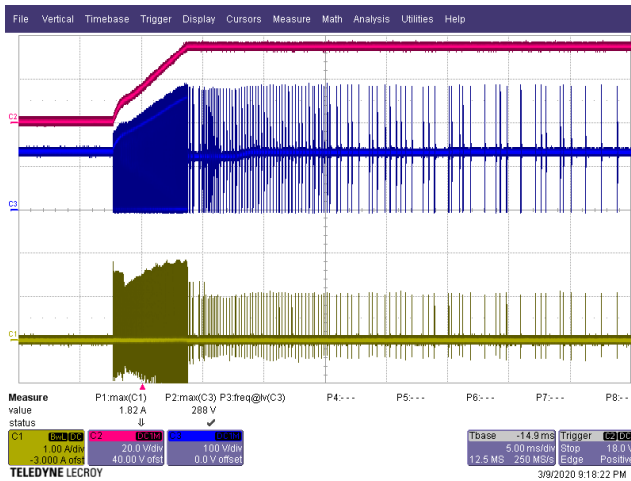
**Figure 440 2** – Flyback Start-up Waveforms, 115 VAC Input, 2 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 100 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 1 A, 5 ms / div.



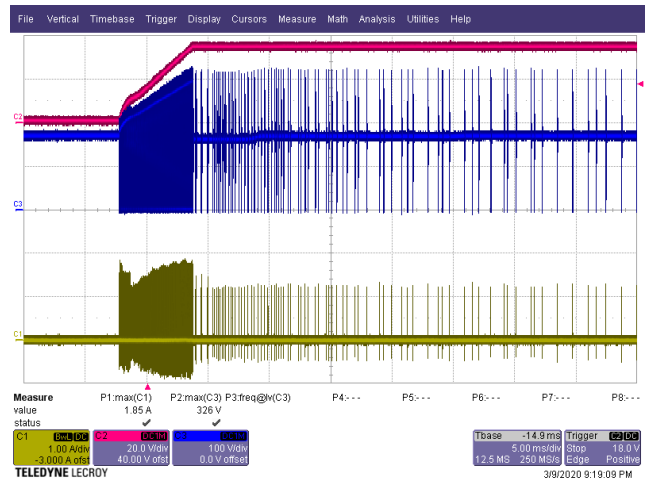
**Figure 41** – Flyback Start-up Waveforms, 230 VAC Input, 2 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 200 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 2 A, 5 ms / div.



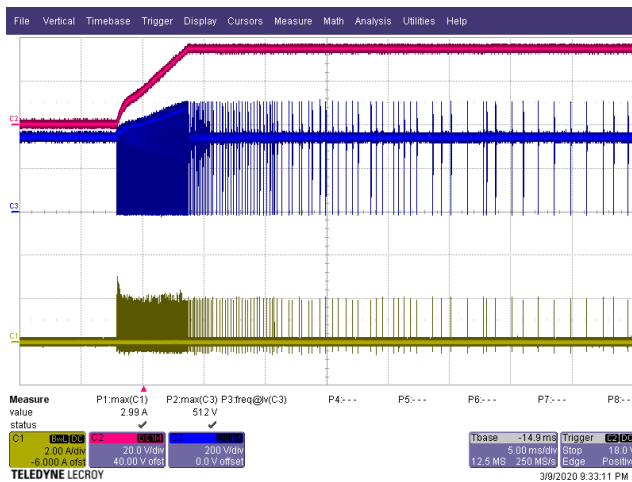
**Figure 42** – Flyback Start-up Waveforms, 264 VAC Input, 2 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 200 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 2 A, 5 ms / div.



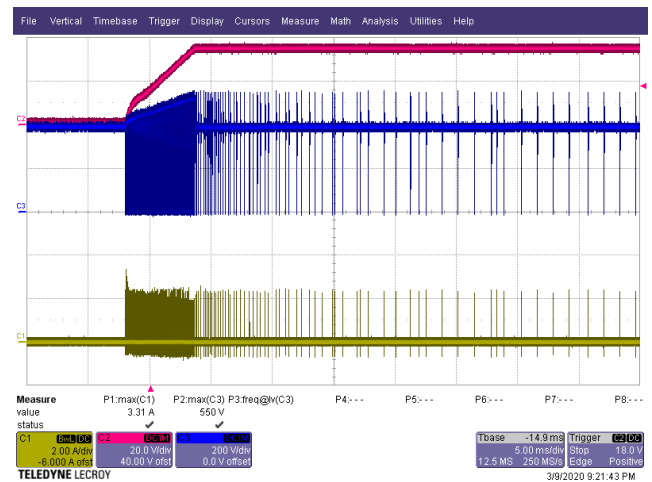
**Figure 43** – Flyback Start-up Waveforms, 90 VAC Input, 0 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 100 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 1 A, 5 ms / div.



**Figure 44** – Flyback Start-up Waveforms, 115 VAC Input, 0 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 100 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 1 A, 5 ms / div.



**Figure 45** – Flyback Start-up Waveforms, 230 VAC Input, 0 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 200 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 2 A, 5 ms / div.



**Figure 46** – Flyback Start-up Waveforms, 264 VAC Input, 0 A Load.  
 Red –  $V_{OUT}$ , 20 V / div.  
 Blu –  $U3 V_{DRAIN}$ , 200 V / div.  
 Yel –  $U3 I_{DRAIN}$ , 2 A, 5 ms / div.

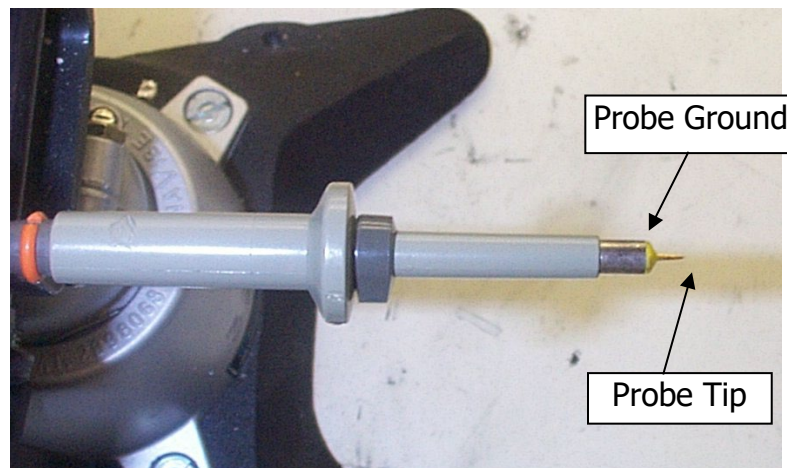


## 12.3 Output Ripple Measurements

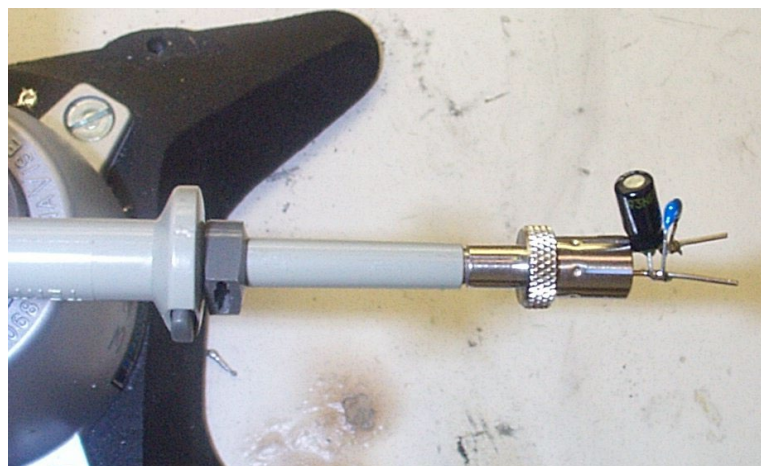
### 12.3.1 Ripple Measurement Technique

For DC output ripple measurements, a modified oscilloscope test probe must be utilized in order to reduce spurious signals due to pick-up. Details of the probe modification are provided in the Figures below.

The 4987BA probe adapter is affixed with two capacitors tied in parallel across the probe tip. The capacitors include one (1) 0.1  $\mu\text{F}/50\text{ V}$  ceramic type and one (1) 47  $\mu\text{F}/50\text{ V}$  aluminum electrolytic. The aluminum electrolytic type capacitor is polarized, so proper polarity across DC outputs must be maintained (see below).



**Figure 47** – Oscilloscope Probe Prepared for Ripple Measurement. (End Cap and Ground Lead Removed)

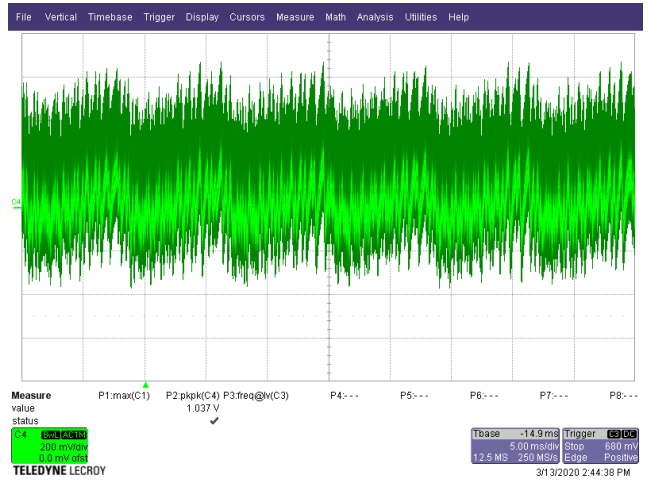


**Figure 48** – Oscilloscope Probe with Probe Master ([www.probemaster.com](http://www.probemaster.com)) 4987A BNC Adapter. (Modified with wires for ripple measurement, and two parallel decoupling capacitors added)

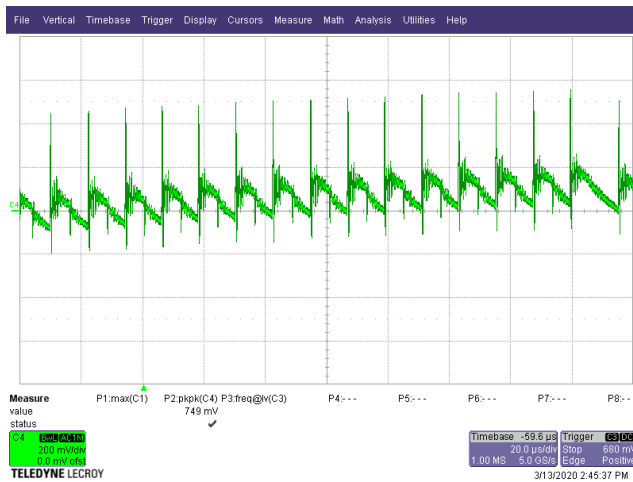
### 12.3.1.1 Output Ripple waveforms



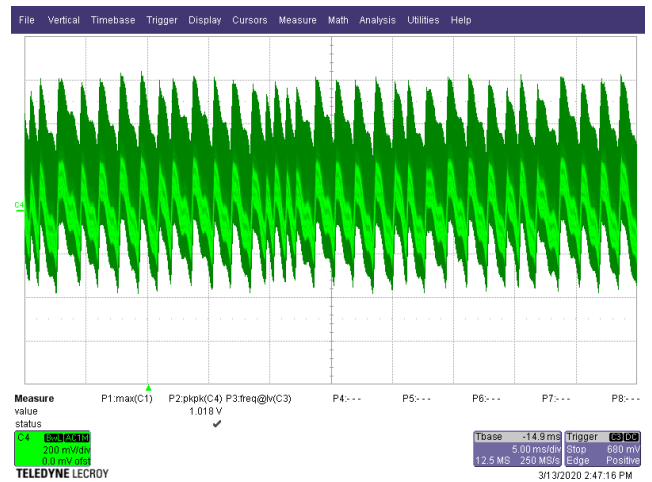
**Figure 49** – Output Ripple. 90 VAC, 2 A Load  
5 ms / 200 m V / div.



**Figure 50** – Output Ripple. 115 VAC, 2 A Load  
5 ms / 200 m V / div.

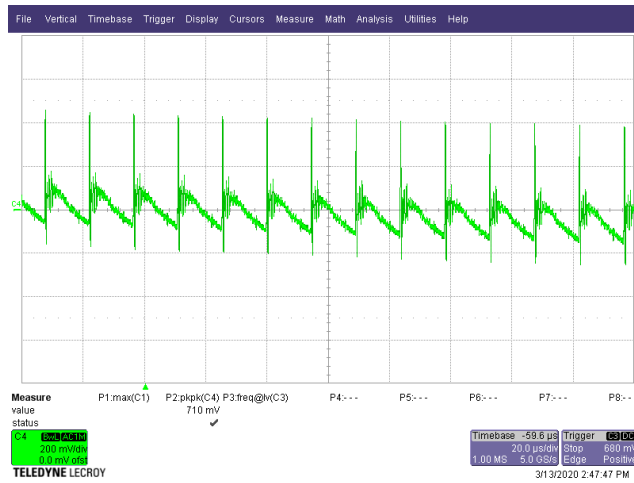


**Figure 51** – Output Ripple, Detail, 115 VAC,  
2 A Load - 20 μs / 200 m V / div.



**Figure 52** – Output Ripple. 230 VAC, 2 A Load  
5 ms / 200 m V / div.



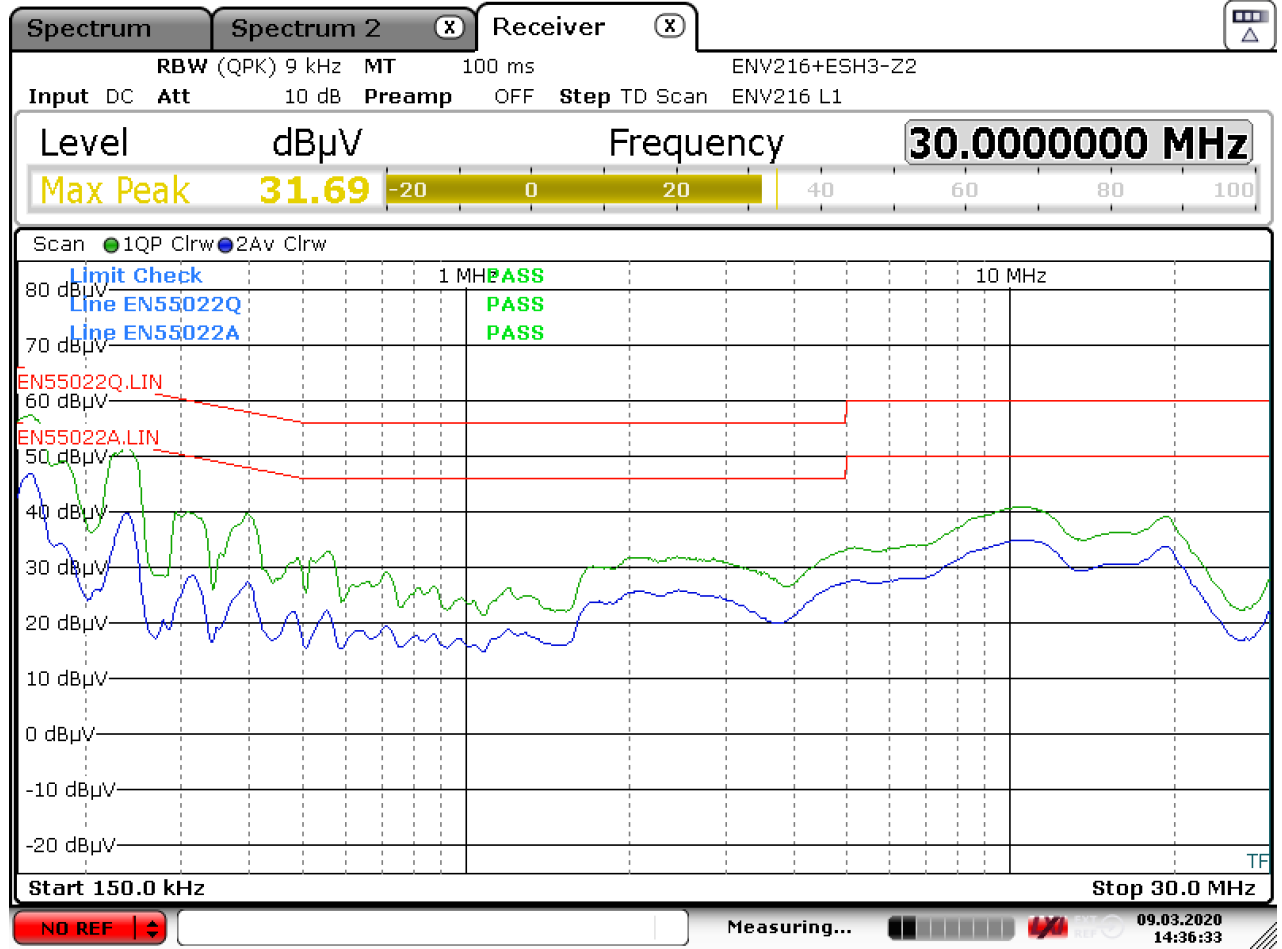


**Figure 53** – Output Ripple, Detail, 230 VAC, 2 A Load  
- 20  $\mu$ s / 200 m V / div.



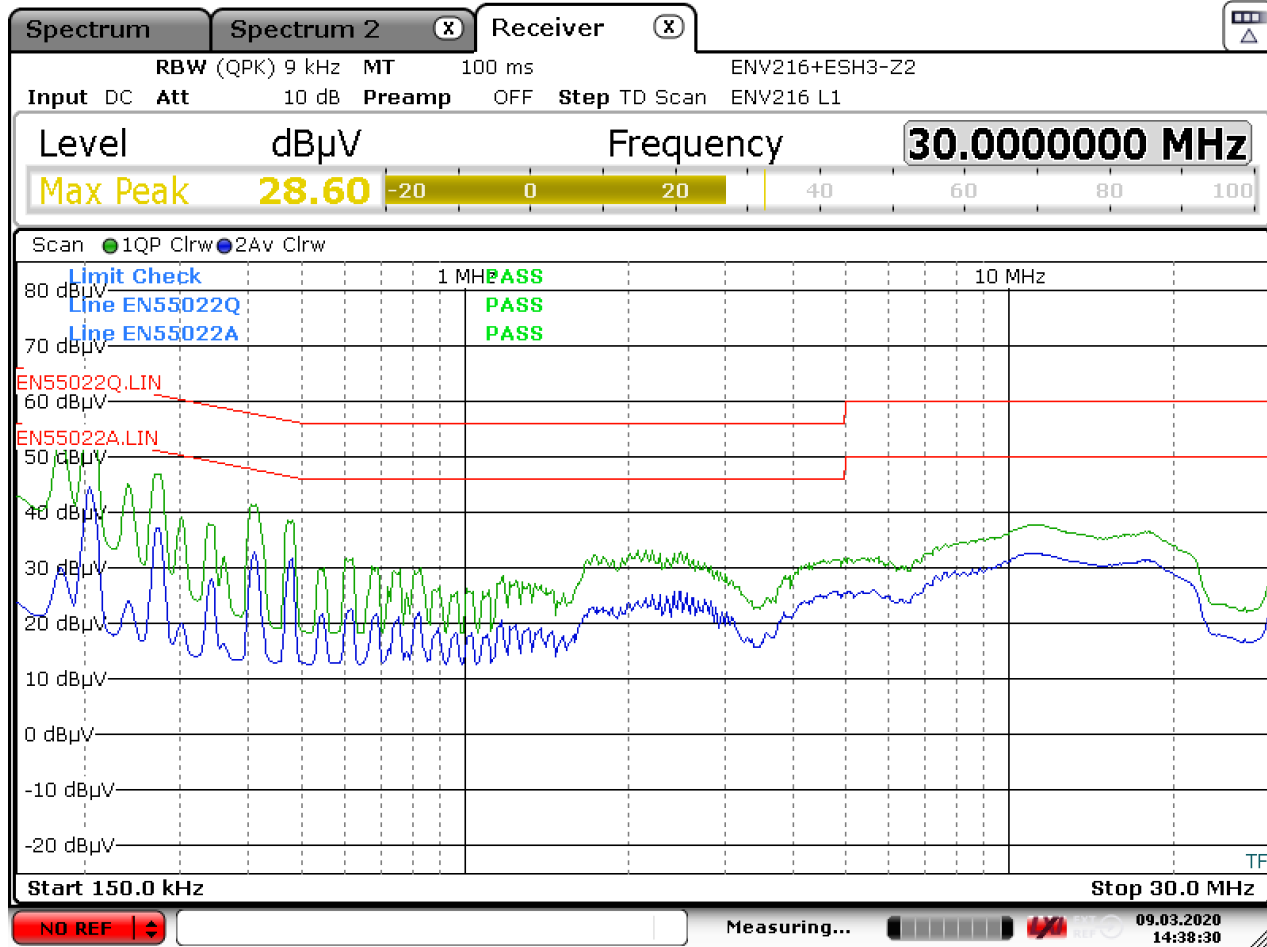
### 13 Conducted EMI

EMI scans were made using an 18Ω resistive load, with the output return grounded to the LISN.



**Figure 54** – EMI, Full Load, 115 VAC, LISN grounded to secondary return.





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Figure 55 – EMI, Full Load, 230 VAC, LISN grounded to secondary return.

## 14 Line Surge

### 14.1 Combination Wave Differential Mode Test

Pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
115	+1	90	2	10	PASS
115	-1	90	2	10	PASS
115	+1	270	2	10	PASS
115	-1	270	2	10	PASS
115	+1	0	2	10	PASS
115	-1	0	2	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance (Ω)	Number of Strikes	Test Result
230	+1	90	2	10	PASS
230	-1	90	2	10	PASS
230	+1	270	2	10	PASS
230	-1	270	2	10	PASS
230	+1	0	2	10	PASS
230	-1	0	2	10	PASS

## 14.2 *Combination Wave Common Mode Test*

Pass criterion is no output interruption.

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance ( $\Omega$ )	Number of Strikes	Test Result
115	+2	90	12	10	PASS
115	-2	90	12	10	PASS
115	+2	270	12	10	PASS
115	-2	270	12	10	PASS
115	+2	0	12	10	PASS
115	-2	0	12	10	PASS

AC Input Voltage (VAC)	Surge Voltage (kV)	Phase Angle (°)	Generator Impedance ( $\Omega$ )	Number of Strikes	Test Result
230	+2	90	12	10	PASS
230	-2	90	12	10	PASS
230	+2	270	12	10	PASS
230	-2	270	12	10	PASS
230	+2	0	12	10	PASS
230	-2	0	12	10	PASS

## 15 ESD

Pass criterion is no permanent output interruption.

### 15.1 Air Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
115	+15	Output +	10	PASS
115	-15	Output -	10	PASS
115	+15	Output +	10	PASS
115	-15	Output -	10	PASS

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+15	Output +	10	PASS
230	-15	Output -	10	PASS
230	+15	Output +	10	PASS
230	-15	Output -	10	PASS

### 15.2 Contact Discharge

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
115	+8.8	Output +	10	PASS
115	-8.8	Output -	10	PASS
115	+8.8	Output +	10	PASS
115	-8.8	Output -	10	PASS

AC Input Voltage (VAC)	Discharge Voltage (kV)	Discharge Point	Number of Strikes	Test Result
230	+8.8	Output +	10	PASS
230	-8.8	Output -	10	PASS
230	+8.8	Output +	10	PASS
230	-8.8	Output -	10	PASS

## 16 Revision History

Date	Author	Revision	Description & Changes	Reviewed
02-Mar-21	RH	5.0	Initial Release.	Apps & Mktg
04-Apr-21	Rh	5.1	Various Text Edits	Apps & Mktg



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