General Purpose Base Board for Gate Driver Core 2SC0115T

Application	General purpose drives, UPS, solar power and others
Specification	Suitable for IGBT power modules in various housings Up to 800V DC-link voltage Electrical interfaces Advanced Active Clamping Short-circuit detection
Author	High-Power Application Engineering Department
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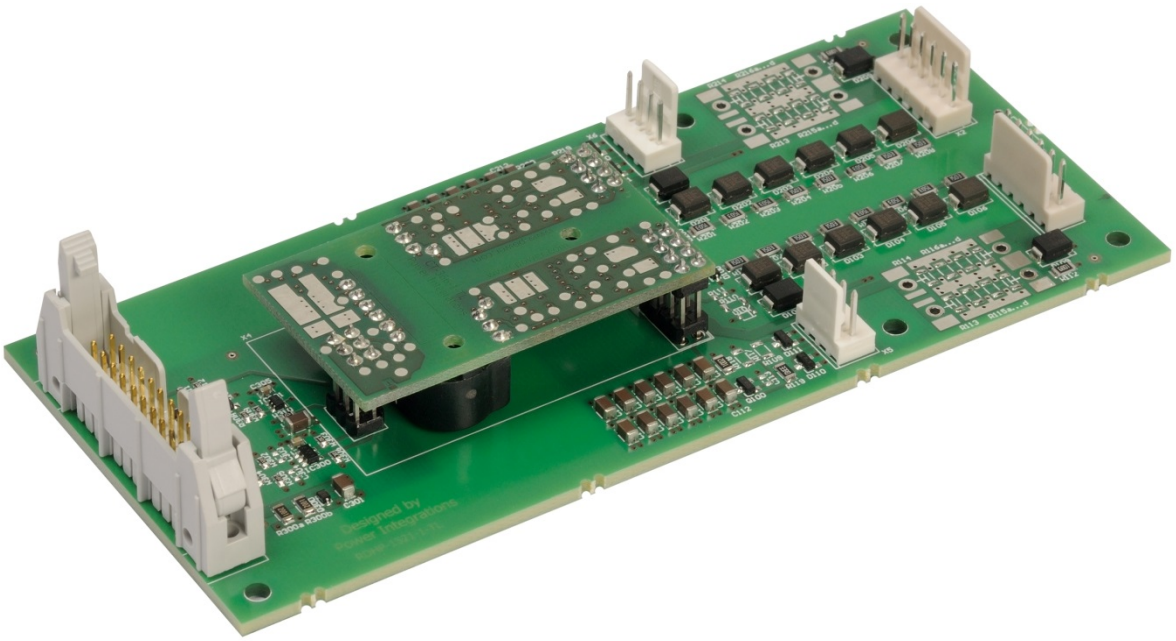

[1] The letter refers to the hardware revision. The number refers to the documentation revision.

Scope

This application proposal provides a circuit design for a general purpose base board for driving various IGBT power modules.

The main features of the design are:

- Suitable for IGBT power modules in various housings such as 17mm dual, 17mm six-pack, 62mm, PrimePACK™, etc. with a maximum blocking voltage of 1200V
- Advanced Active Clamping
- Short-circuit detection
- Electrical command inputs and status outputs
- Secondary side fault inputs (optional)
- Secondary side status feedback outputs (optional)
- 0V/15V command input logic
- 0V/15V status output logic
- Minimum pulse suppression (optional)
- Adjustable blocking time
- 15V supply voltage
- Single PCB solution with soldered-in gate driver core

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Application Conditions

The design is proposed for the following application conditions:

- General purpose applications and IGBT power modules
- Adaptations such as adjustment of gate resistors can easily be done

Design Description

In addition to the following design description, reference to the datasheet(s) and application manual of the 2SC0115T gate driver family is recommended.

Gate Resistors

Gate resistor values are not explicitly given as they depend on the IGBT power module used and on the application. Gate resistors of either SMD (size 1206) or THT (size PR02) package can be selected.

Turn-on gate resistors:

Channel	SMD Package	THT Package
1	R116a … R116d	R114
2	R216a … R216d	R214

Turn-off gate resistors:

Channel	SMD Package	THT Package
1	R115a … R115d	R113
2	R215a … R215d	R213

The gate resistors must be determined and assembled by the user. Minimum required gate resistor values are defined in the datasheet of the gate driver 2SC0115T.

V_{CEsat} Monitoring

In the schematic and bill of material, the resistor networks of the V_{CEsat} monitoring function are marked with "N.A." (not assembled), as their concrete value depends on the IGBT power module and applied DC-link voltage.

Recommended values are listed in the following table:

IGBT voltage	Max. DC-link voltage	R100	R101 to R108	R200	R201 to R208
600V	400V	62kΩ	82kΩ	62kΩ	82kΩ
1200V	800V	120kΩ	150kΩ	120kΩ	150kΩ

Recommended values of the blanking capacitors C100 and C200 as well as further details of the V_{CEsat} monitoring function are described in the corresponding application manual of the gate driver 2SC0115T.

Soft Shut Down (SSD)

For this design proposal no dedicated Soft Shut Down function is implemented. Instead, for over voltage protection Active Clamping is implemented.

Advanced Active Clamping

Active clamping is a technique designed to partially turn on the IGBT in case the collector-emitter voltage exceeds a predefined threshold. The IGBT is then kept in linear operation. Basic Active Clamping topologies

implement a single feedback path from the IGBT's collector through transient voltage suppressor (TVS) diodes to the IGBT gate.

Advanced active clamping topologies implement the same structure as basic active clamping topologies, but in addition a fraction of the active clamping current is fed into the gate driver core at pins ACLx via 20Ω resistors. In this case, when active clamping is activated, the turn-off MOSFET of the 2SC0115T driver is switched off in order to improve the effectiveness of the active clamping and to reduce the losses in the TVS diodes. This feature – called Advanced Active Clamping – is mainly integrated in the secondary-side ASIC of gate driver core 2SC0115T.

In the schematic and bill of material, the TVS networks (D101 to D106 and D201 to D206) are marked with "N.A." (not assembled), as their specific value depends on the IGBT power module and applied DC-link voltage. Recommended values are listed in the following tables.

IGBT voltage	Max. DC-link voltage	D108, D208	D101 … D105, D201 … D205	D106, D206
600V	400V	STPS340U	P6SMBJ70A	P6SMBJ70CA
1200V	800V	STPS340U	SMBJ130A-E3	SMBJ130CA-E3

For further details and alternative TVS diodes refer to the application manual of the gate driver core 2SC0115T.

Minimum Pulse Suppression

This design possesses the option to implement a minimum pulse suppression with a time constant τ. If required the minimum pulse suppression can be set by adjusting C303 and C304. The time constant τ is given by the following equations:

$\tau_1 = 0.88k\Omega \cdot C303$

$\tau_2 = 0.88k\Omega \cdot C304$

Recommended values of C303 and C304 are in the range of 100pF (τ_x = 88ns) to 470pF (τ_x = 414ns), depending on actual application conditions.

Blocking Time

During the blocking time the gate driver ignores incoming command signals. The blocking time starts once a fault was detected by the gate driver's secondary side (undervoltage lock-out or a short-circuit event) or when an undervoltage condition ends on the primary side.

The terminal TB allows the default blocking time of typically 99ms (R312) to be reduced by connecting an optional external resistor to GND. The external resistor R_b needs to be equal or larger than 129kΩ to fulfill the following formula:

$(R_b + 6.8k\Omega) \,||\, 150k\Omega \triangleq T_b + 51ms$ with $20ms < T_b < 99ms$

In case the terminal TB is directly shorted to GND (R_b = 0Ω), the blocking time is set to its minimum value as descripted in the datasheet of the gate driver core 2SC0115T.

Secondary Side Fault Inputs

When the terminals FLT1 (channel 1) and/or FLT2 (channel 2) are set to a positive voltage (according to the following table), the driver detects an external fault condition. The connected IGBT is then turned off immediately. The minimum holding time for applying the positive voltage is described in the datasheet and application manual of the gate driver core 2SC0115T.

Depending on the desired positive voltage level at the fault inputs an optional voltage divider can be realized at the terminals of FTL1 (R109) and FLT2 (R209). Recommended values are:

Fault input voltage level (referenced to COM1/COM2)	R109	R209
5V	33Ω	33Ω
10V	33Ω	33Ω
15V	2.2kΩ	2.2kΩ
24V	6.8kΩ	6.8kΩ

The capacitors C113 and C213 may be used to implement filtering at the inputs. The time constant τ is given by the following equation:

$\tau = Cx13 \cdot (Rx09 \cdot 4.7k\Omega) / (Rx09 + 4.7k\Omega)$

If required, the recommended values of C113 and C213 are in the range of 100pF to 470pF, depending on application conditions. Note that the minimum holding time for applying the positive voltage at the inputs will be increased accordingly.

Secondary Side Status Feedback Output

In normal operation each edge of the control signal at INA and INB, respectively, is acknowledged by the driver with a short pulse, which is available at the corresponding terminal ACK1 and/or ACK2 (for details refer to the 2SC0115T application manual).

In addition the following fault conditions are also shown at the terminals ACK1 and/or ACK2:

- The terminal ACK1/ACK2 is pulled to COM1/COM2 for a period of typically 9µs once a V_{CE} desaturation is detected.
- During a secondary-side supply undervoltage the terminal ACK1/ACK2 is pulled to COM1/COM2 as long as the undervoltage condition remains. Note that during power-up, ACK1/ACK2 will also show a fault condition until the supply undervoltage disappears.
- As long as an external fault is present at the terminals FLT1 and/or FLT2, ACK1/ACK2 will be pulled to COM1/COM2.

Interfaces

Electrical Interfaces

X3		
Pin	Designation	Description
1	n.c.	Not connected
3	n.c.	Not connected
5	VCC	15V supply (referenced to GND)
7	VCC	15V supply (referenced to GND)
9	n.c.	Not connected
11	INB	Command input channel 2
13	SO	Combined status output
15	INA	Command input channel 1
17	n.c.	Not connected
19	TB	Set blocking time

X3		
Pin	Designation	Description
2	GND	Ground
4	GND	Ground
6	GND	Ground
8	GND	Ground
10	GND	Ground
12	GND	Ground
14	GND	Ground
16	GND	Ground
18	GND	Ground
20	GND	Ground

X1		
Pin	Designation	Description
1	C1	Collector channel 1
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	G1	Gate channel 1
6	VE1	Emitter channel 1

X2		
Pin	Designation	Description
1	C2	Collector channel 2
2	n.c.	Not connected
3	n.c.	Not connected
4	n.c.	Not connected
5	G2	Gate channel 2
6	VE2	Emitter channel 2

X5		
Pin	Designation	Description
1	VISO1	24V supply (referenced to COM1)
2	FLT1	Fault input channel 1
3	ACK1	Acknowledge channel 1
4	COM1	Ground channel 1

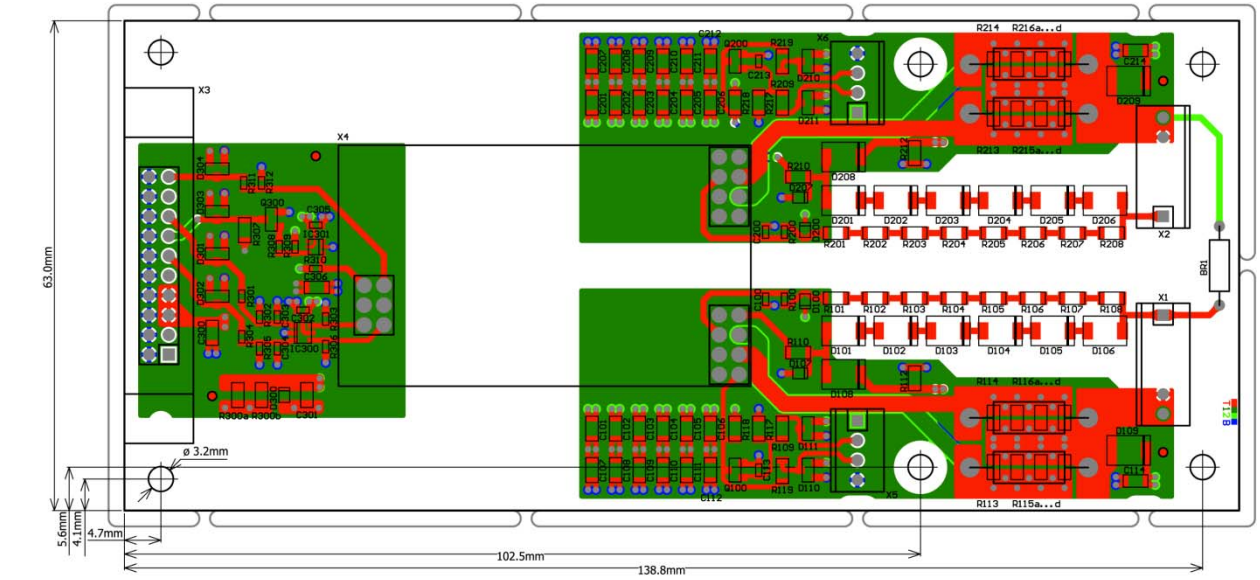
X6		
Pin	Designation	Description
1	VISO2	24V supply (referenced to COM2)
2	FLT2	Fault input channel 2
3	ACK2	Acknowledge channel 2
4	COM2	Ground channel 2

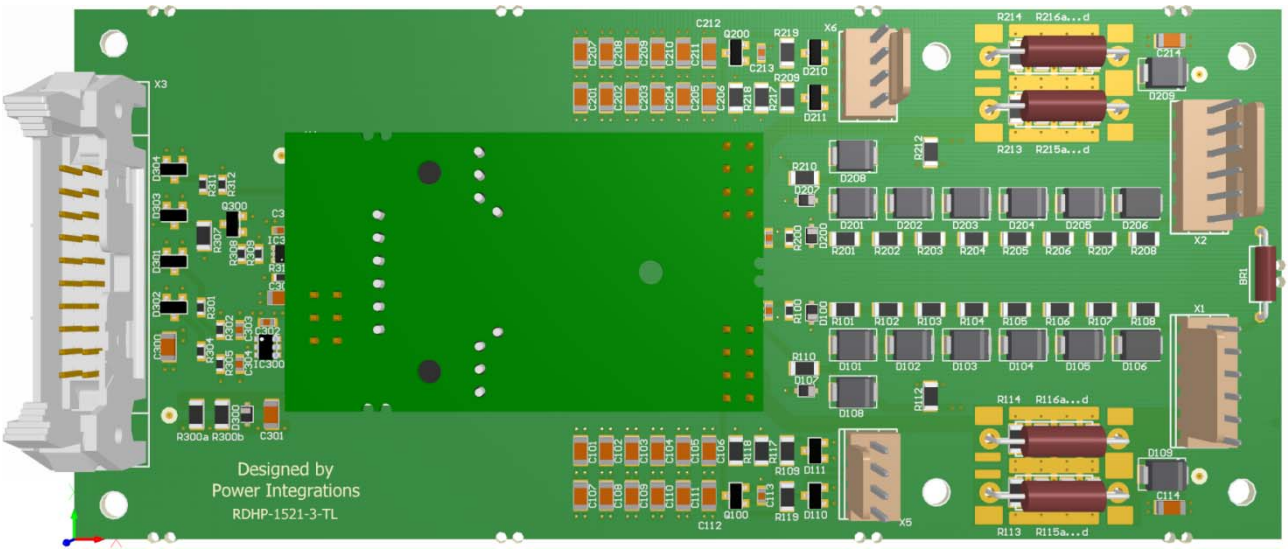
CAD Data

The set of CAD data, which includes the circuit schematics, Gerber files, BOM and Pick-and-Place file are available as separate documents bundled together with this documentation.

Layout Example

An example for a suitable layout is shown in the following picture. The recommended PCB thickness is 1.55mm.





Switching Characteristic

Turn-On / Off

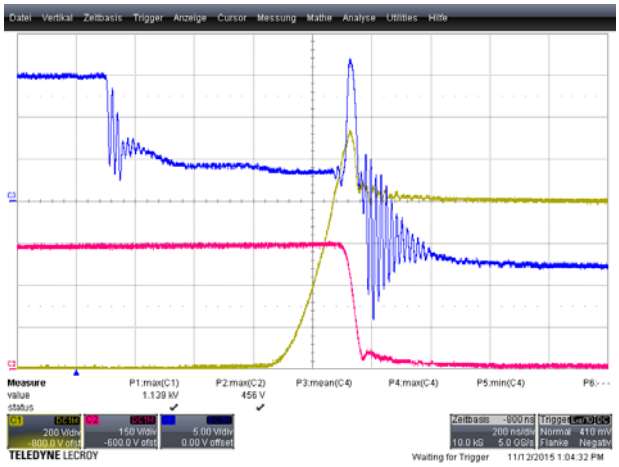
The measurement examples shown with the IGBT power module FF450R12KE4 from Infineon Technologies (R_{Gon} = 4.3Ω and R_{Goff} = 4.3Ω) were carried out in a double-pulse test using a half-bridge topology setup at room temperature with an initial DC-link voltage of 800V_{DC}. The adjusted load current is either 450A (I_{nom}) or 900A (2x I_{nom}).

Channel assignment:

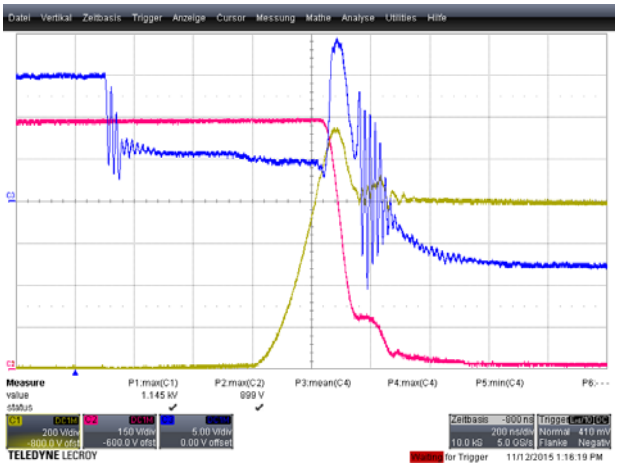
Channel C1: Collector-emitter voltage

Channel C2: Collector current (1V ≙ 1A)

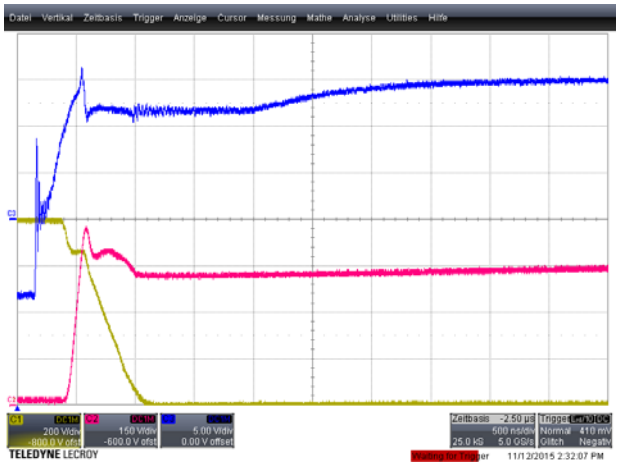
Channel C3: Gate-emitter voltage



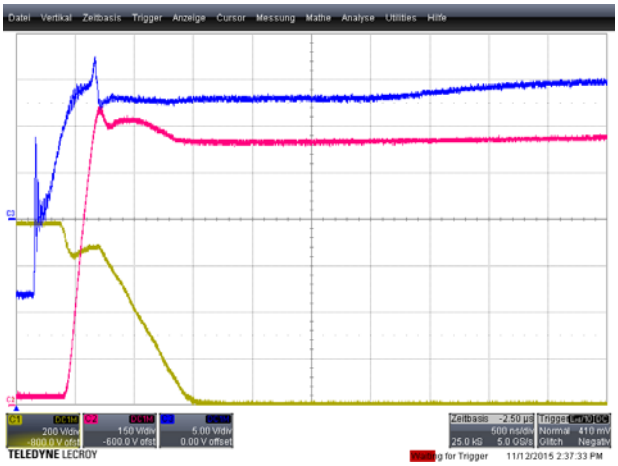
Turn-off bottom side (I_{nom})



Turn-off bottom side (2x I_{nom})



Turn-on bottom side (I_{nom})



Turn-on bottom side (2x I_{nom})

Short-Circuit

The measurement example shown with the IGBT power module FF450R12KE4 from Infineon Technologies (R_{Gon} = 4.3Ω and R_{Goff} = 4.3Ω) was carried out at room temperature with an initial DC-link voltage of 800V_{DC}.

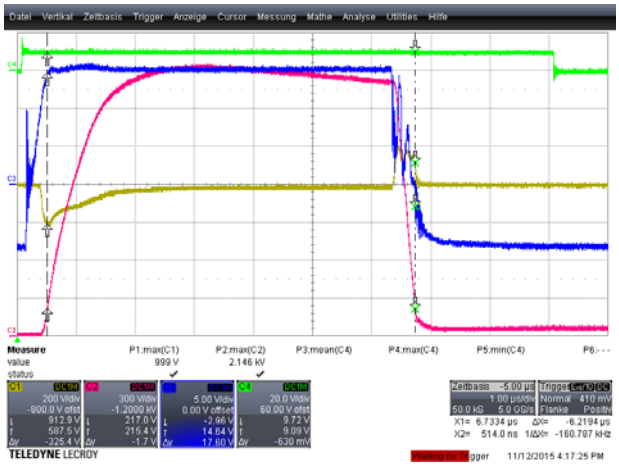
Channel assignment:

Channel C1: Collector-emitter voltage

Channel C2: Collector current (1V ≙ 1A)

Channel C3: Gate-emitter voltage

Channel C4: Command input signal



Bottom side

Handling

To avoid possible failures caused by ESD, a handling- and assembly-process with persistent ESD protection is necessary /3/.

References

/1/ 2SC0115T2xx-12 Data Sheet, Power Integrations

/2/ 2SC0115T2xx-12 Description & Application Manual, Power Integrations

/3/ Application Note AN-0902, "Avoiding ESD with CONCEPT Drivers", Power Integrations

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